FIG. 12

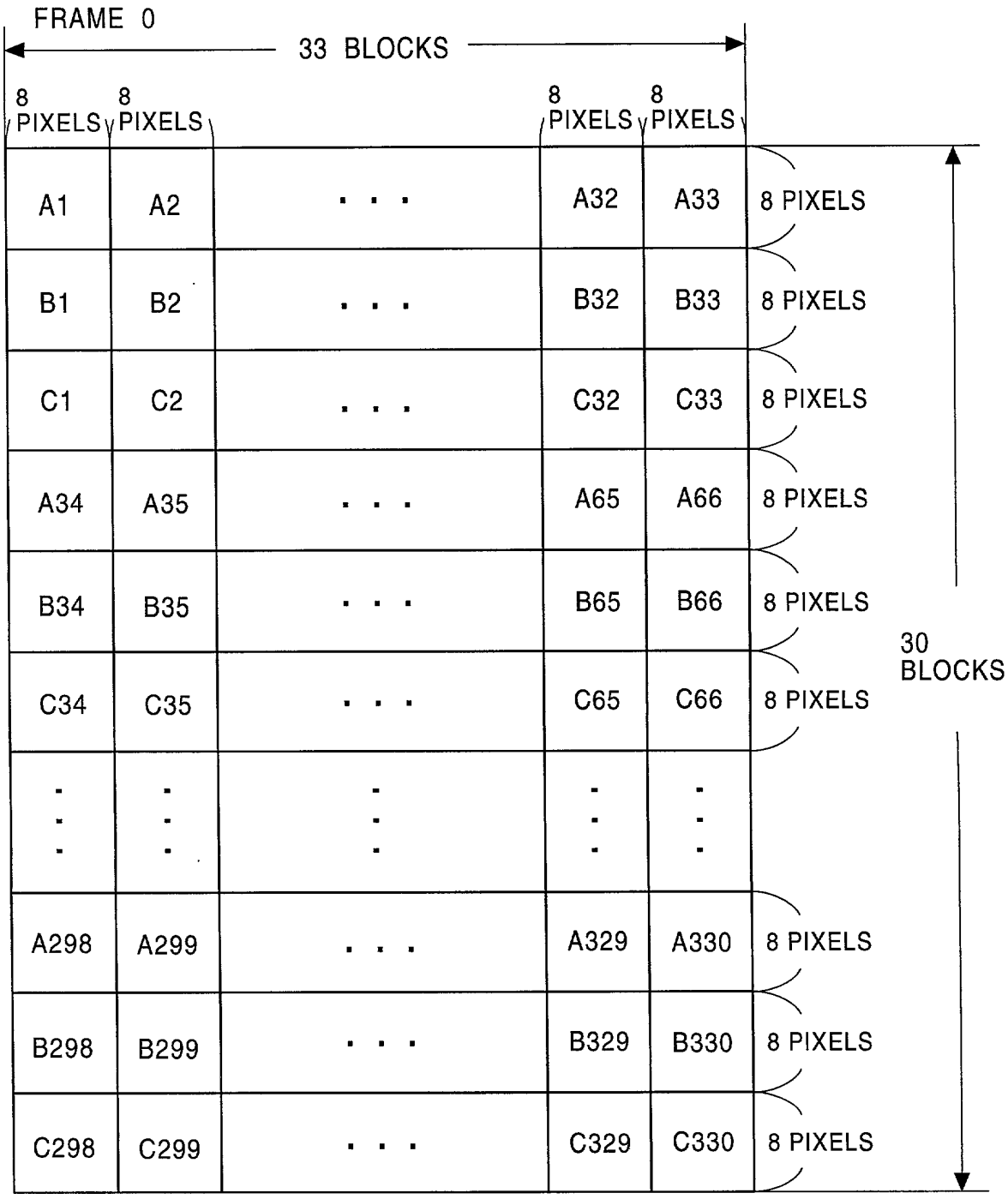

FRAME 0
33 BLOCKS
8 PIXELS
8 PIXELS
8 PIXELS
8 PIXELS
A1
A2
A32
A33
8 PIXELS
B1
B2
B32
B33
8 PIXELS
C1
C2
C32
C33
8 PIXELS
A34
A35
A65
A66
8 PIXELS
B34
B35
B65
B66
8 PIXELS
C34
C35
C65
C66
8 PIXELS
30 BLOCKS
A298
A299
A329
A330
8 PIXELS
B298
B299
B329
B330
8 PIXELS
C298
C299
C329
C330
8 PIXELS

FIG. 13

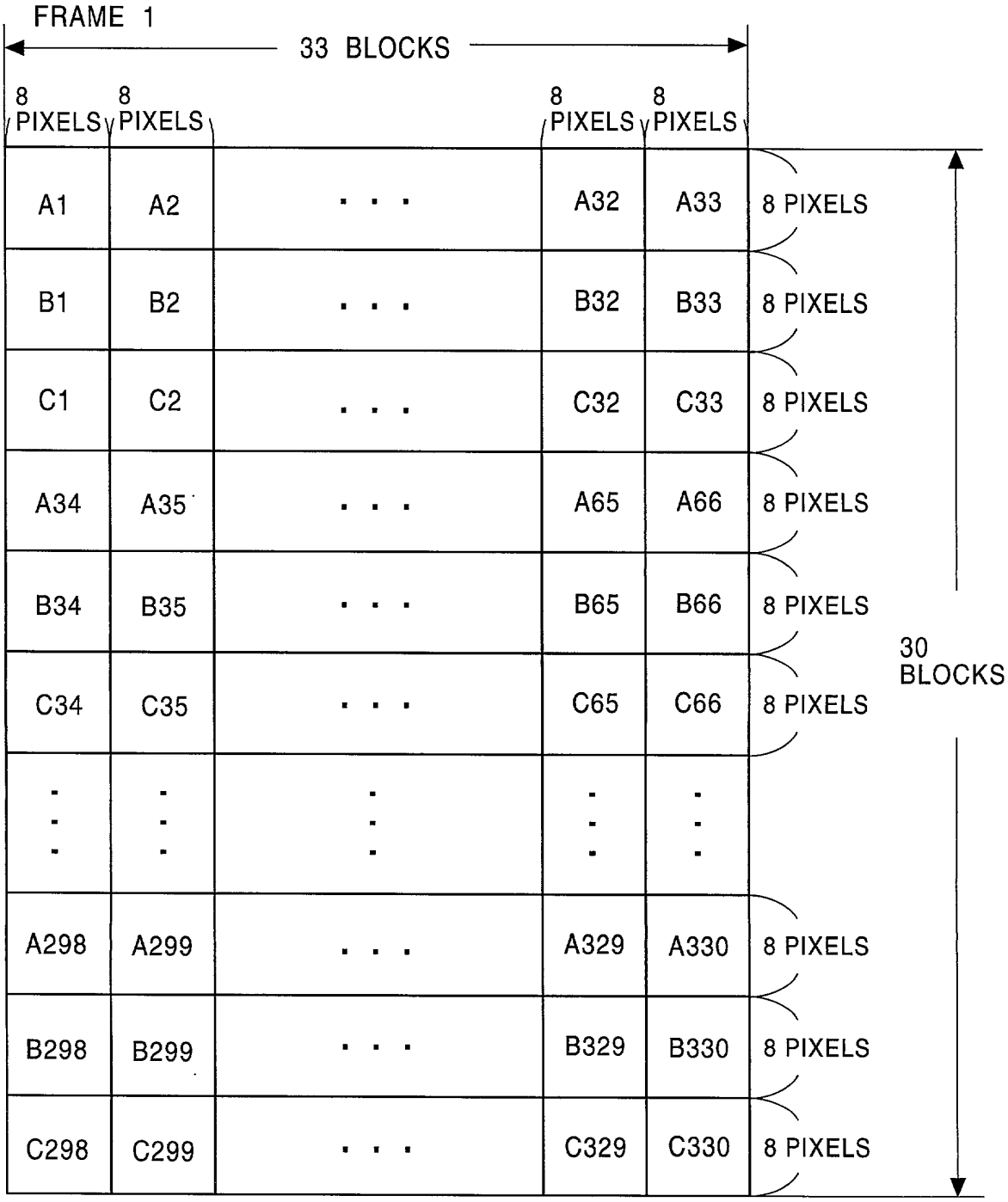

FRAME 1
33 BLOCKS
8 PIXELS
8 PIXELS
8 PIXELS
8 PIXELS
A1
A2
A32
A33
B1
B2
B32
B33
C1
C2
C32
C33
A34
A35
A65
A66
B34
B35
B65
B66
C34
C35
C65
C66
A298
A299
A329
A330
B298
B299
B329
B330
C298
C299
C329
C330
8 PIXELS
30 BLOCKS

FIG. 14

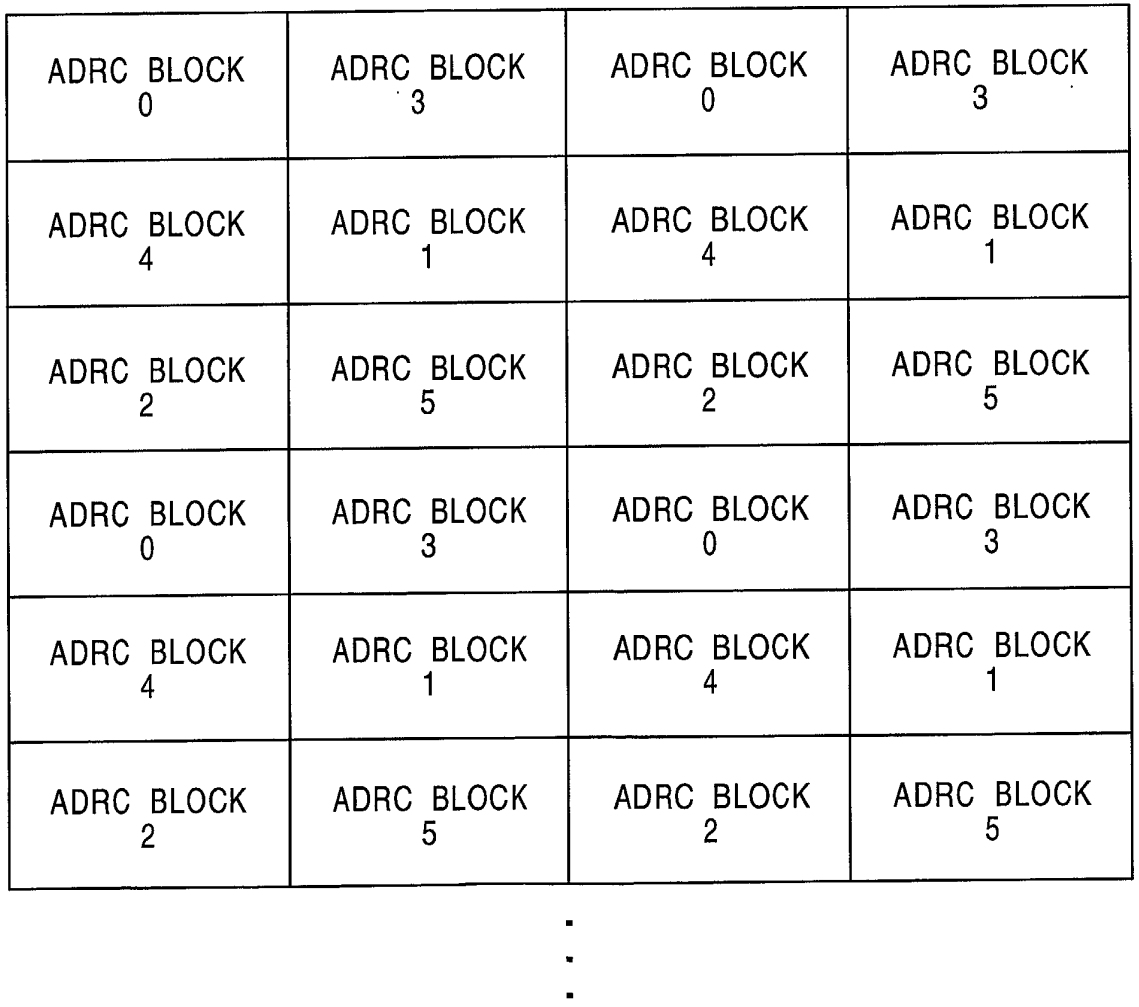

ADRC BLOCK 0
ADRC BLOCK 3
ADRC BLOCK 0
ADRC BLOCK 3
ADRC BLOCK 4
ADRC BLOCK 1
ADRC BLOCK 4
ADRC BLOCK 1
ADRC BLOCK 2
ADRC BLOCK 5
ADRC BLOCK 2
ADRC BLOCK 5
ADRC BLOCK 0
ADRC BLOCK 3
ADRC BLOCK 0
ADRC BLOCK 3
ADRC BLOCK 4
ADRC BLOCK 1
ADRC BLOCK 4
ADRC BLOCK 1
ADRC BLOCK 2
ADRC BLOCK 5
ADRC BLOCK 2
ADRC BLOCK 5

FIG. 15A

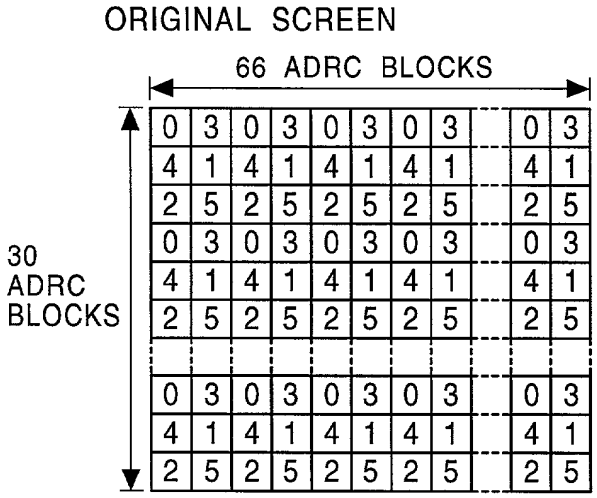


FIG. 15B

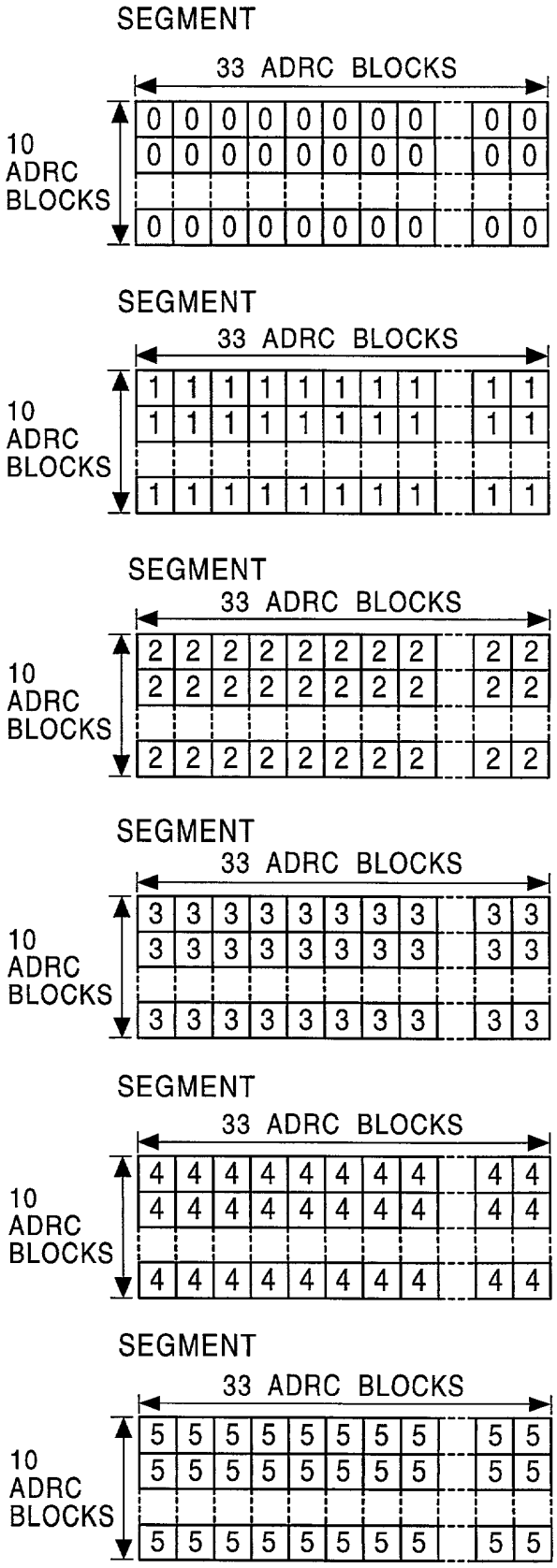


FIG. 16A

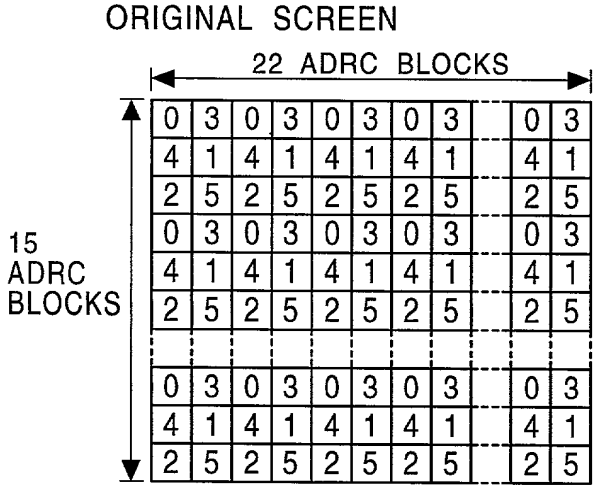


FIG. 16B

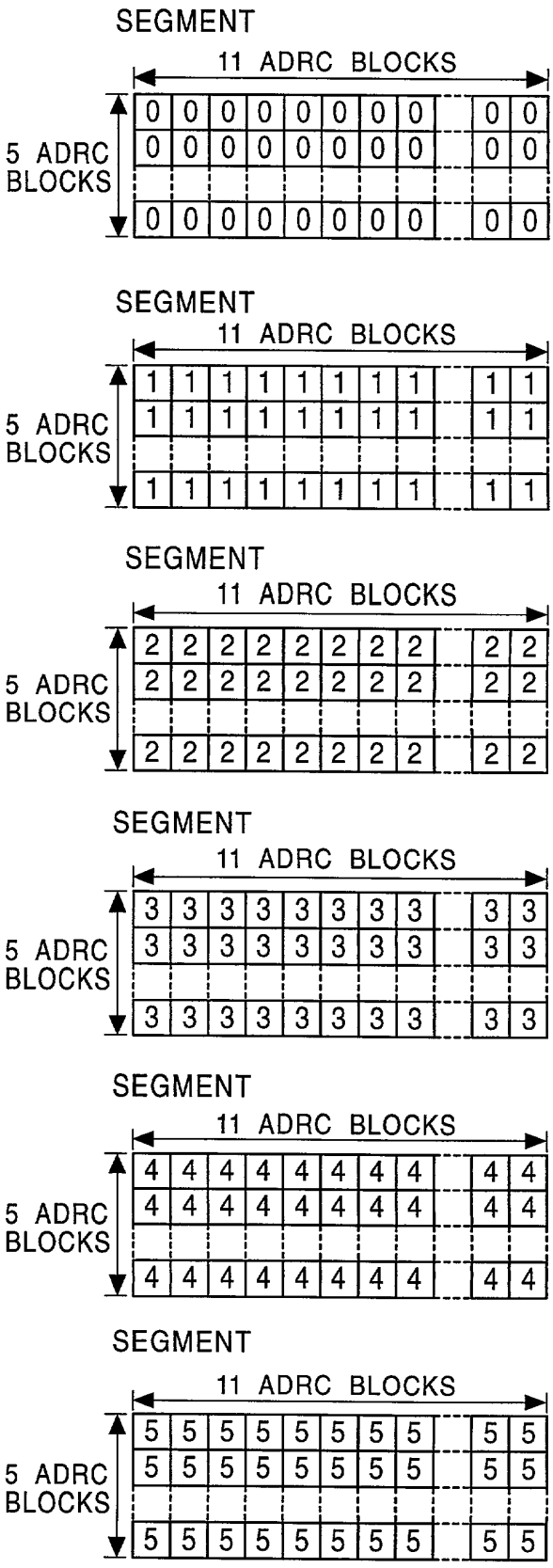


FIG. 17A

y0	y1	y2	y3	y4		y32
y33	y34	y35	y36	y37		y65
y297	y298	y299	y300	y301		y329

FIG. 17B

y0	y221	y112	y3	y224		y142
y33	y254	y145	y36	y257		y175
y297	y188	y79	y300	y191		y109

FIG. 17C

u0	u1	u2	u3	u4		u10
u11	u12	u13	u14	u15		u21
u44	u45	u46	u47	u48		u54

FIG. 17D

u54	u53	u52	u51	u50		u44
u43	u42	u41	u40	u39		u33
u10	u9	u8	u7	u6		u0

FIG. 17E

v0	v1	v2	v3	v4		v10
v11	v12	v13	v14	v15		v21
v44	v45	v46	v47	v48		v54

FIG. 17F

v54	v53	v52	v51	v50		v44
v43	v42	v41	v40	v39		v33
v10	v9	v8	v7	v6		v0

FIG. 18

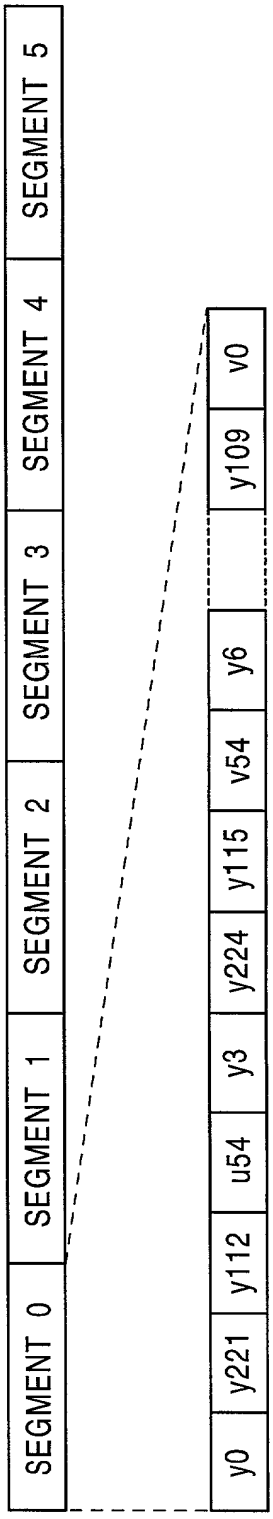

SEGMENT 0
SEGMENT 1
SEGMENT 2
SEGMENT 3
SEGMENT 4
SEGMENT 5
y0
y221
y112
u54
y3
y224
y115
v54
y6
y109
v0

FIG. 19

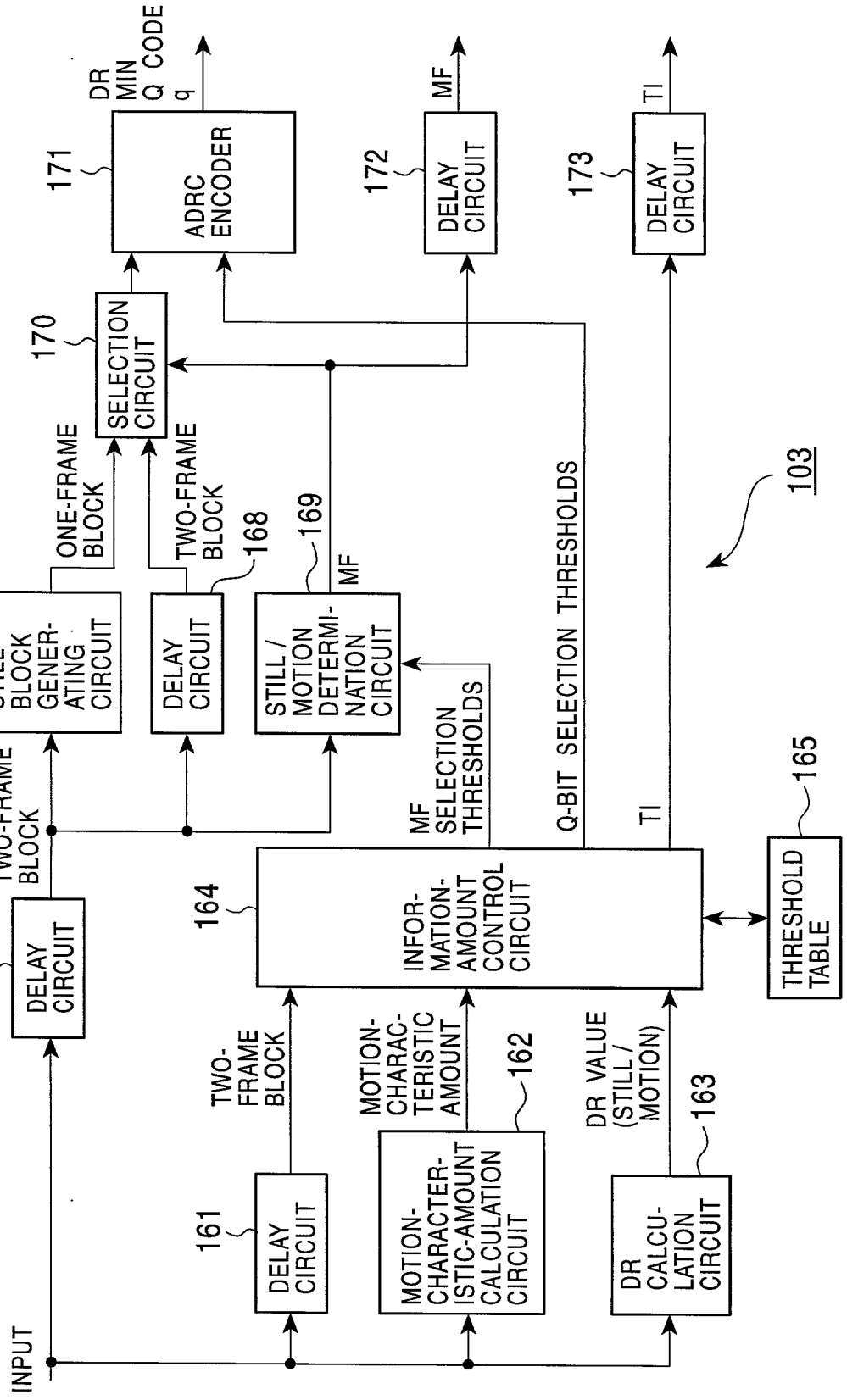

INPUT
DELAY CIRCUIT
161
TWO-FRAME BLOCK
MOTION-CHARACTERISTIC-AMOUNT CALCULATION CIRCUIT
162
MOTION-CHARACTERISTIC AMOUNT
DR CALCULATION CIRCUIT
163
DR VALUE (STILL/MOTION)
INFORMATION-AMOUNT CONTROL CIRCUIT
164
THRESHOLD TABLE
165
DELAY CIRCUIT
166
TWO-FRAME BLOCK
STILL-BLOCK GENERATING CIRCUIT
167
DELAY CIRCUIT
168
STILL/MOTION DETERMINATION CIRCUIT
169
MF
SELECTION CIRCUIT
170
ONE-FRAME BLOCK
TWO-FRAME BLOCK
ADRC ENCODER
171
DR
MIN
Q CODE
q
DELAY CIRCUIT
172
MF
DELAY CIRCUIT
173
TI
MF SELECTION THRESHOLDS
Q-BIT SELECTION THRESHOLDS
TI
103

FIG. 20

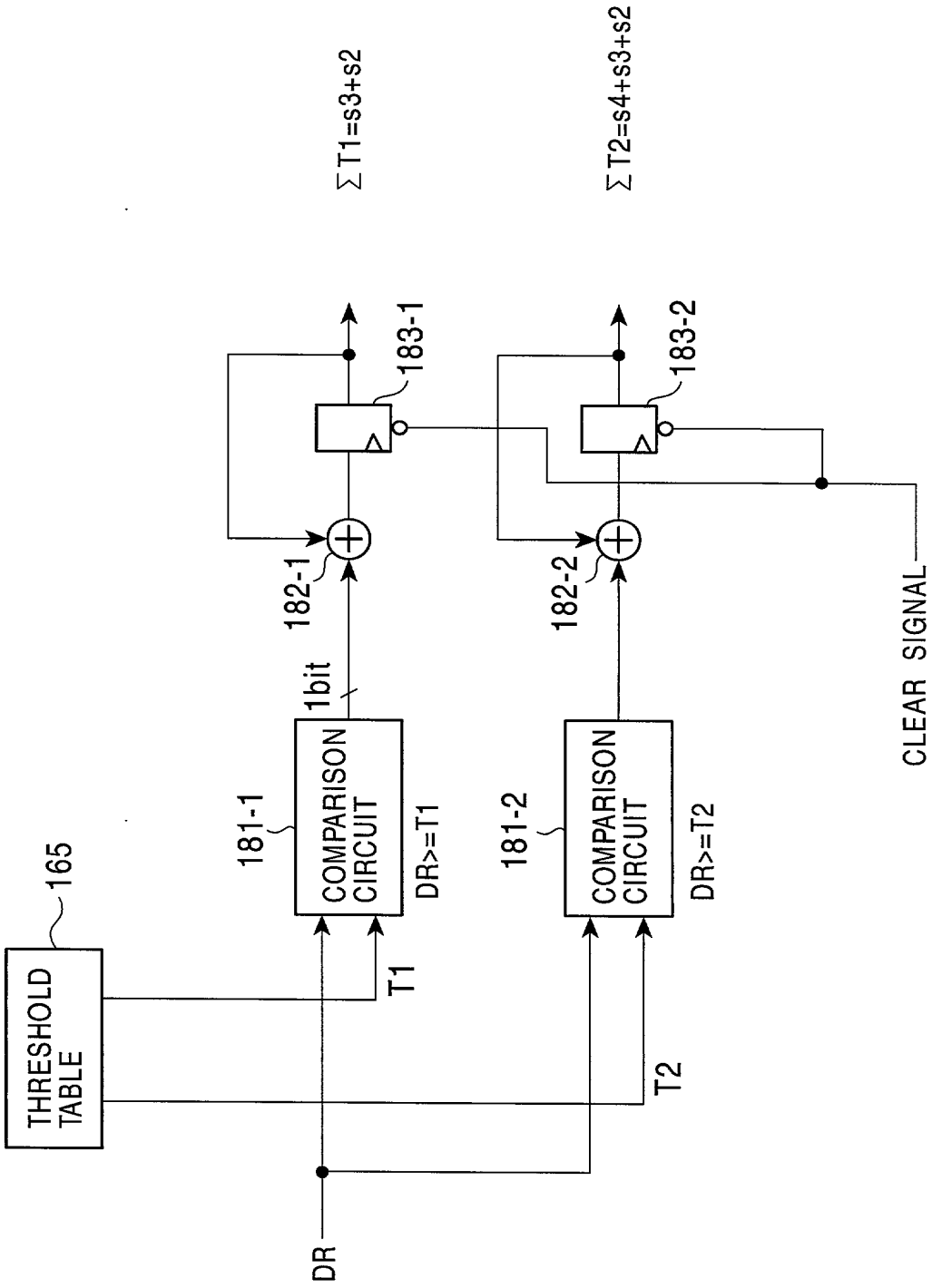

∑T1=s3+s2
∑T2=s4+s3+s2
183-1
183-2
182-1
182-2
1bit
181-1
181-2
COMPARISON CIRCUIT
COMPARISON CIRCUIT
DR>=T1
DR>=T2
165
THRESHOLD TABLE
T1
T2
DR
CLEAR SIGNAL

FIG. 21

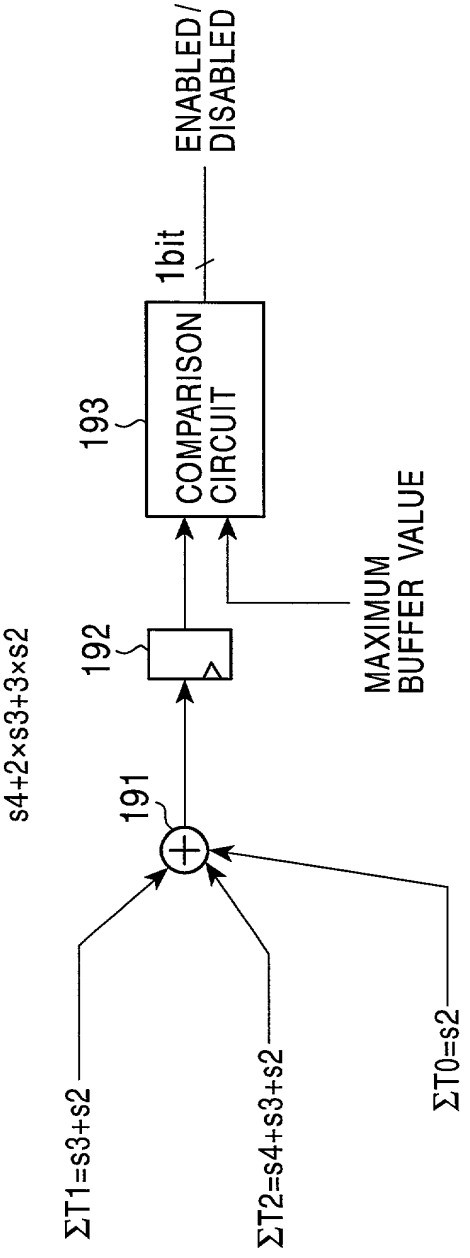

ΣT1=s3+s2
ΣT2=s4+s3+s2
ΣT0=s2
191
s4+2×s3+3×s2
192
193
COMPARISON CIRCUIT
1bit
ENABLED/ DISABLED
MAXIMUM BUFFER VALUE

FIG. 22

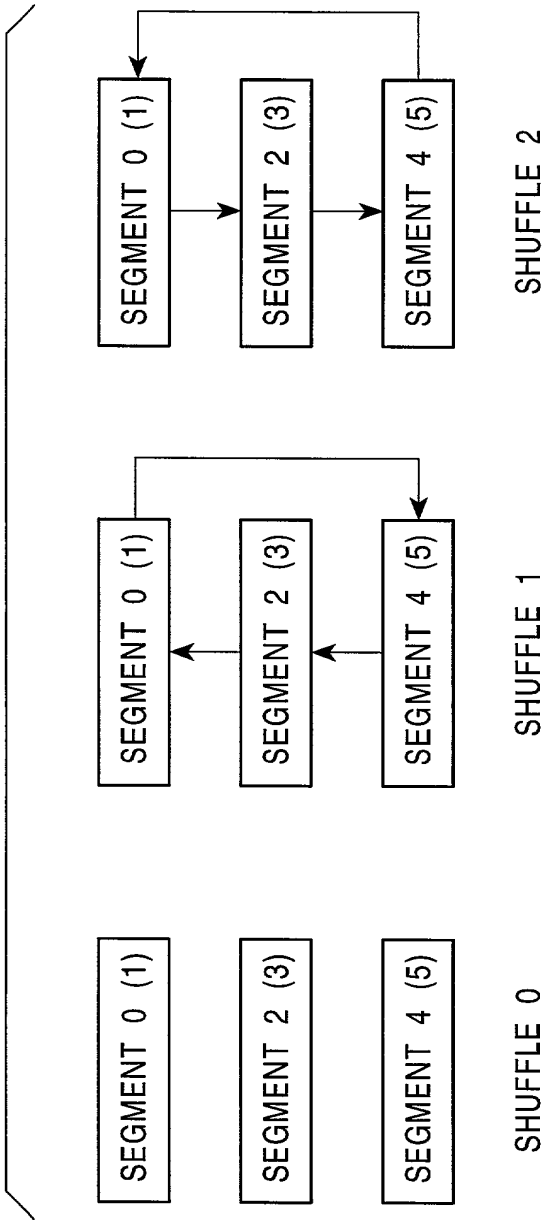

SEGMENT 0 (1)
SEGMENT 2 (3)
SEGMENT 4 (5)
SHUFFLE 0
SEGMENT 0 (1)
SEGMENT 2 (3)
SEGMENT 4 (5)
SHUFFLE 1
SEGMENT 0 (1)
SEGMENT 2 (3)
SEGMENT 4 (5)
SHUFFLE 2

FIG. 23

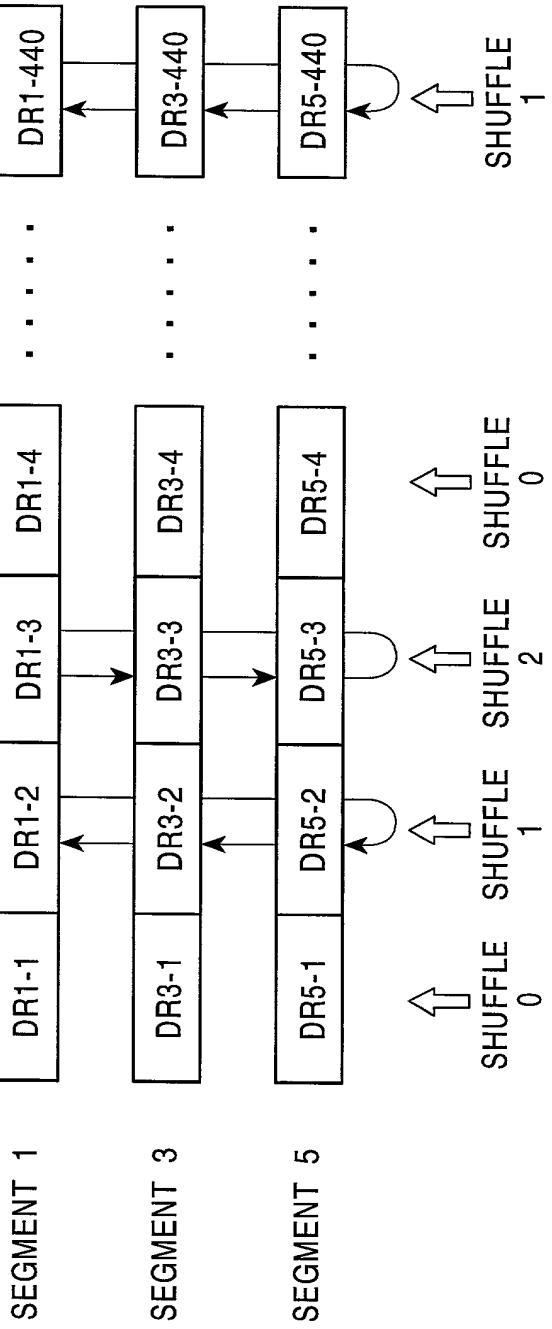

SEGMENT 1
SEGMENT 3
SEGMENT 5
DR1-1
DR1-2
DR1-3
DR1-4
DR3-1
DR3-2
DR3-3
DR3-4
DR5-1
DR5-2
DR5-3
DR5-4
DR1-440
DR3-440
DR5-440
SHUFFLE 0
SHUFFLE 1
SHUFFLE 2
SHUFFLE 0
SHUFFLE 1

FIG. 24

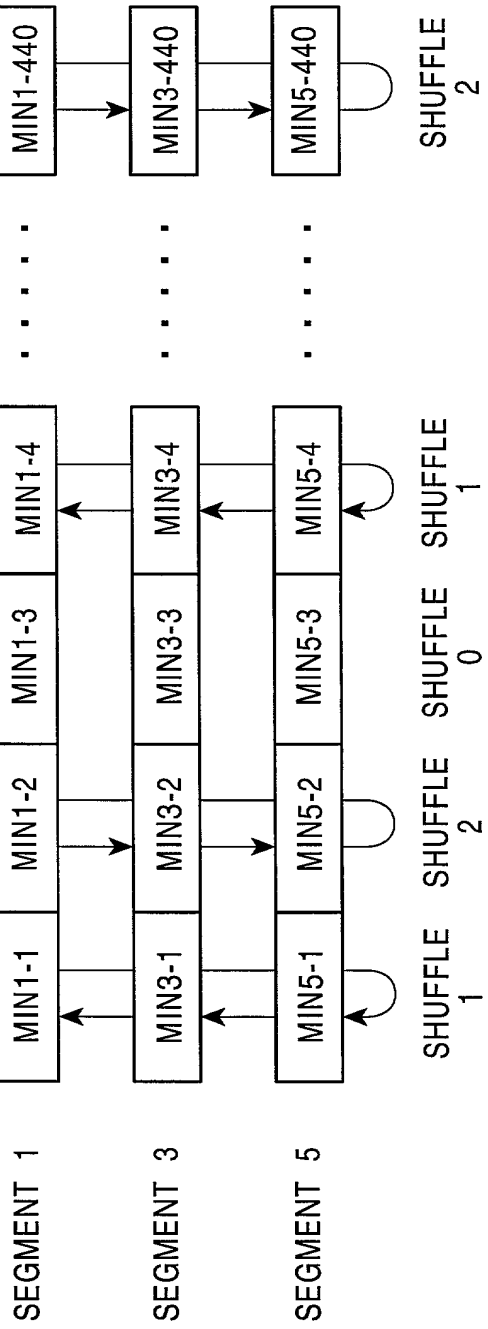

SEGMENT 1
SEGMENT 3
SEGMENT 5
MIN1-1
MIN1-2
MIN1-3
MIN1-4
MIN3-1
MIN3-2
MIN3-3
MIN3-4
MIN5-1
MIN5-2
MIN5-3
MIN5-4
MIN1-440
MIN3-440
MIN5-440
SHUFFLE 1
SHUFFLE 2
SHUFFLE 0
SHUFFLE 1
SHUFFLE 2

FIG. 25

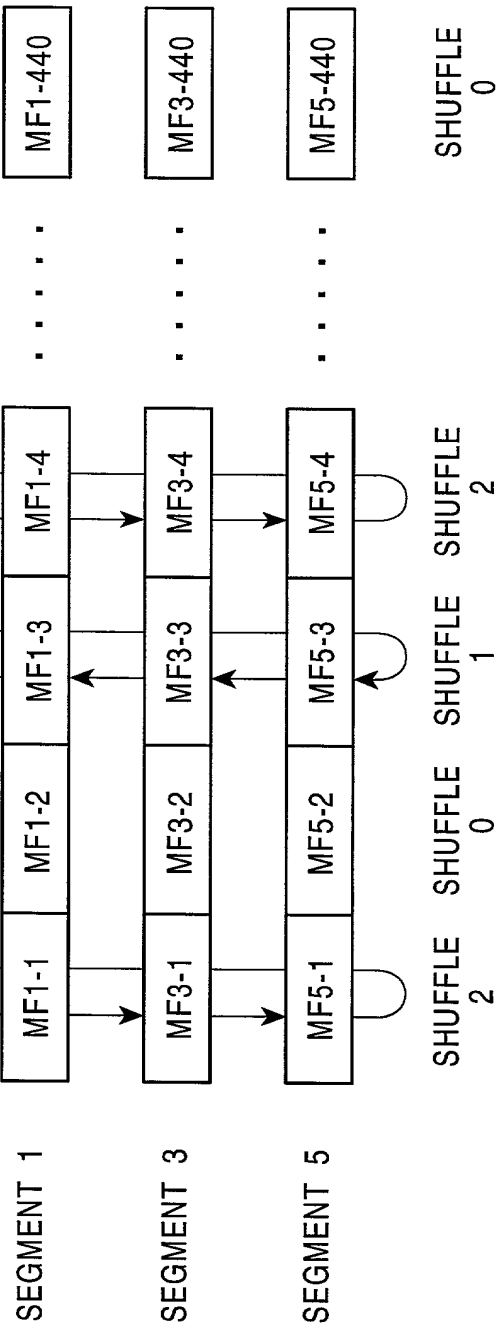

SEGMENT 1
SEGMENT 3
SEGMENT 5
MF1-1
MF1-2
MF1-3
MF1-4
MF1-440
MF3-1
MF3-2
MF3-3
MF3-4
MF3-440
MF5-1
MF5-2
MF5-3
MF5-4
MF5-440
SHUFFLE 2
SHUFFLE 0
SHUFFLE 1
SHUFFLE 2
SHUFFLE 0

FIG. 26

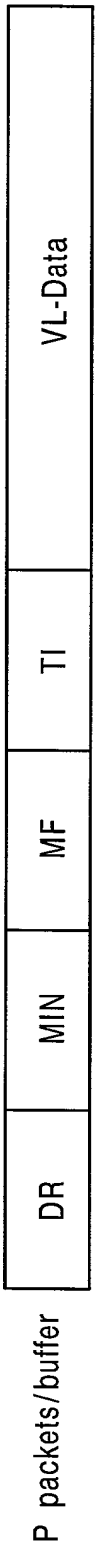

P packets/buffer
DR
MIN
MF
TI
VL-Data
Abit×8M
Bbit×8M
Cbit×8M
Dbit×8M
8bit×N

FIG. 27

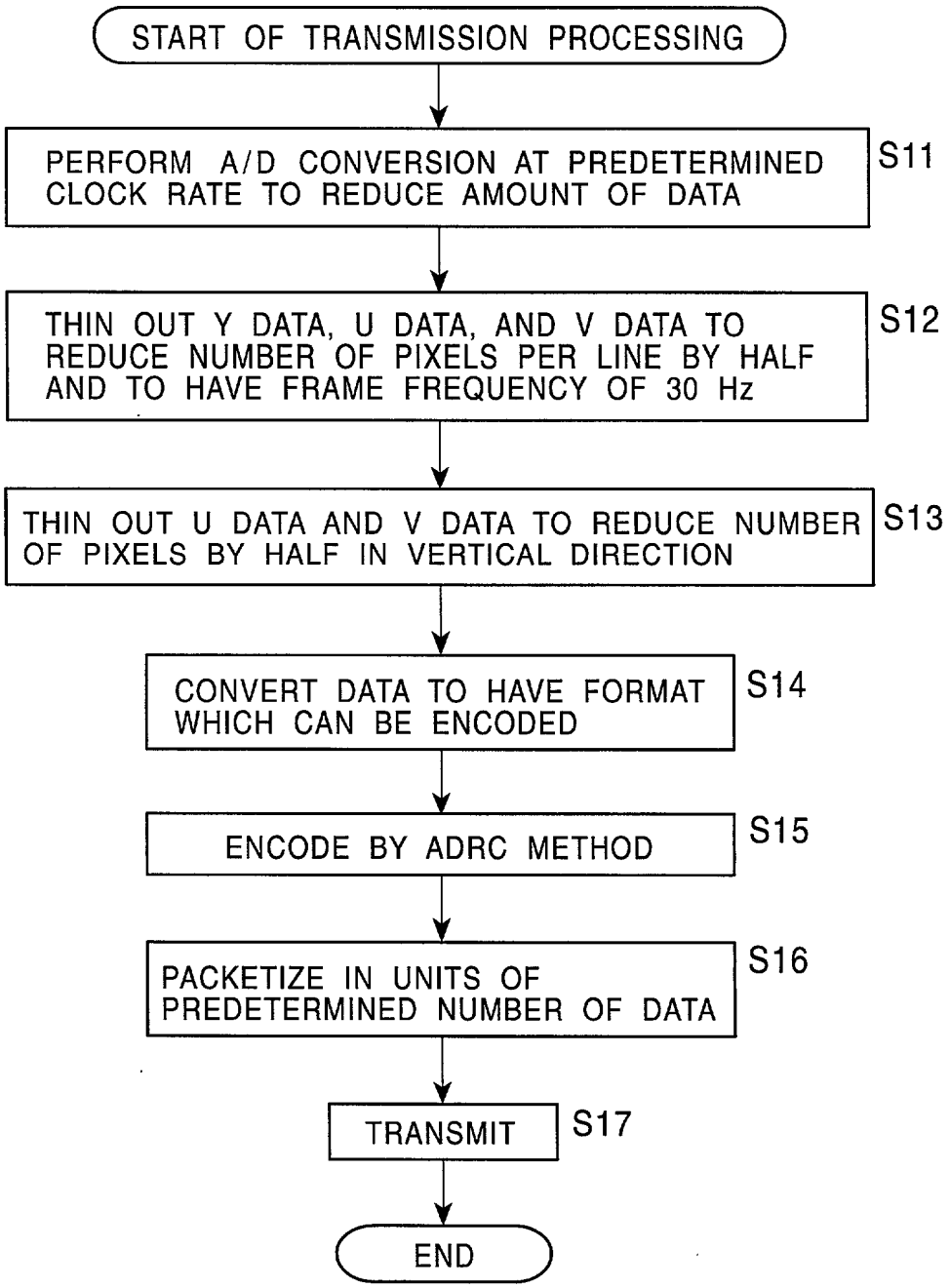

START OF TRANSMISSION PROCESSING
PERFORM A/D CONVERSION AT PREDETERMINED CLOCK RATE TO REDUCE AMOUNT OF DATA
S11
THIN OUT Y DATA, U DATA, AND V DATA TO REDUCE NUMBER OF PIXELS PER LINE BY HALF AND TO HAVE FRAME FREQUENCY OF 30 Hz
S12
THIN OUT U DATA AND V DATA TO REDUCE NUMBER OF PIXELS BY HALF IN VERTICAL DIRECTION
S13
CONVERT DATA TO HAVE FORMAT WHICH CAN BE ENCODED
S14
ENCODE BY ADRC METHOD
S15
PACKETIZE IN UNITS OF PREDETERMINED NUMBER OF DATA
S16
TRANSMIT
S17
END

FIG. 28

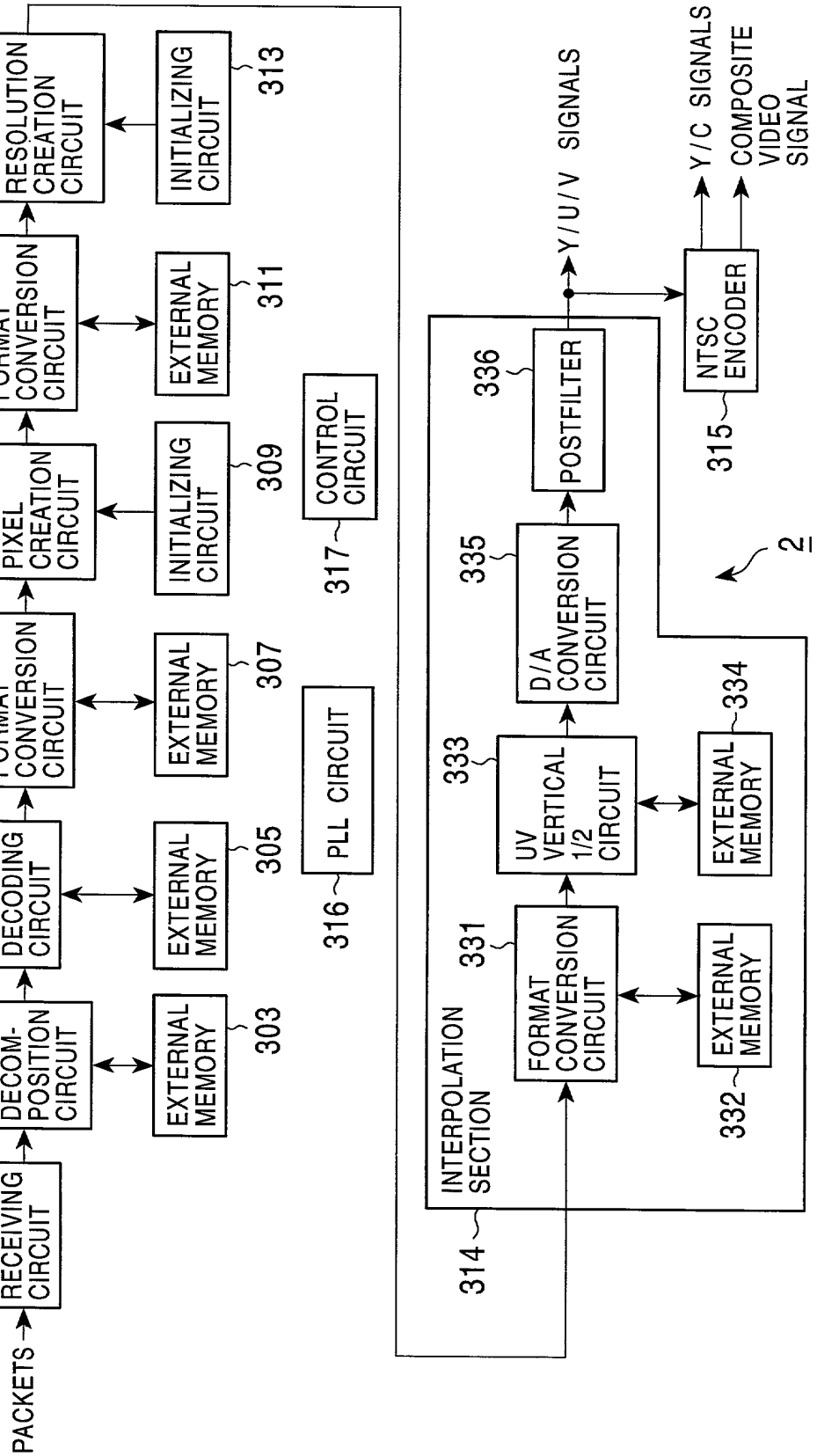

PACKETS
RECEIVING CIRCUIT
301
PACKET DECOM-POSITION CIRCUIT
302
EXTERNAL MEMORY
303
DECODING CIRCUIT
304
EXTERNAL MEMORY
305
FORMAT CONVERSION CIRCUIT
306
EXTERNAL MEMORY
307
MISSING-PIXEL CREATION CIRCUIT
308
INITIALIZING CIRCUIT
309
FORMAT CONVERSION CIRCUIT
310
EXTERNAL MEMORY
311
QUADRUPLE-DENSITY-RESOLUTION CREATION CIRCUIT
312
INITIALIZING CIRCUIT
313
INTERPOLATION SECTION
314
FORMAT CONVERSION CIRCUIT
331
EXTERNAL MEMORY
332
UV VERTICAL 1/2 CIRCUIT
333
EXTERNAL MEMORY
334
D/A CONVERSION CIRCUIT
335
POSTFILTER
336
NTSC ENCODER
315
Y/U/V SIGNALS
Y/C SIGNALS
COMPOSITE VIDEO SIGNAL
PLL CIRCUIT
316
CONTROL CIRCUIT
317
2

FIG. 29

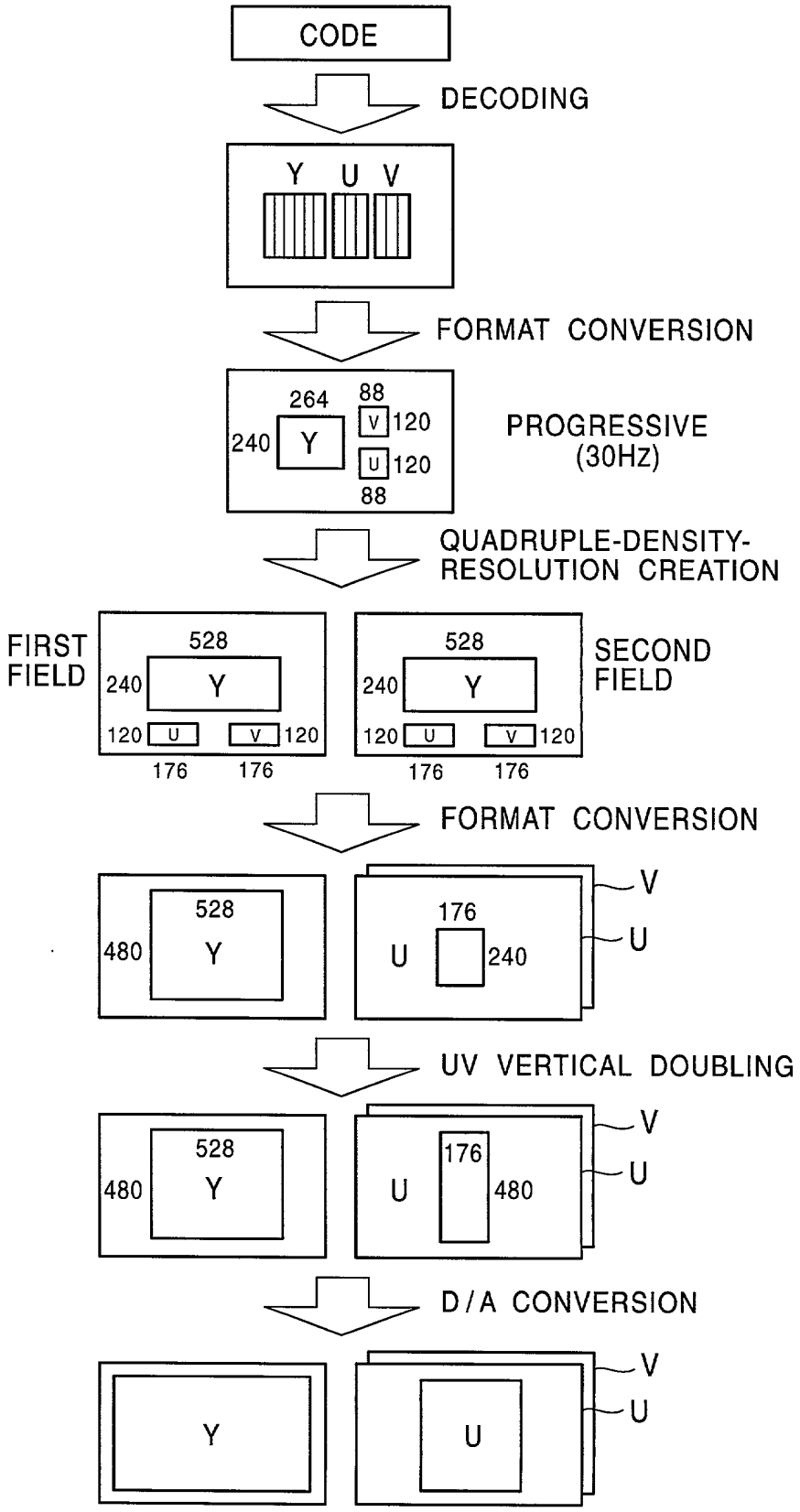

CODE
DECODING
Y U V
FORMAT CONVERSION
264
88
240
Y
V
120
U
120
88
PROGRESSIVE
(30Hz)
QUADRUPLE-DENSITY-
RESOLUTION CREATION
FIRST
FIELD
528
240
Y
120
U
V
120
176
176
528
240
Y
120
U
V
120
176
176
SECOND
FIELD
FORMAT CONVERSION
528
480
Y
176
U
240
V
U
UV VERTICAL DOUBLING
528
480
Y
176
U
480
V
U
D/A CONVERSION
Y
U
V
U

FIG. 30

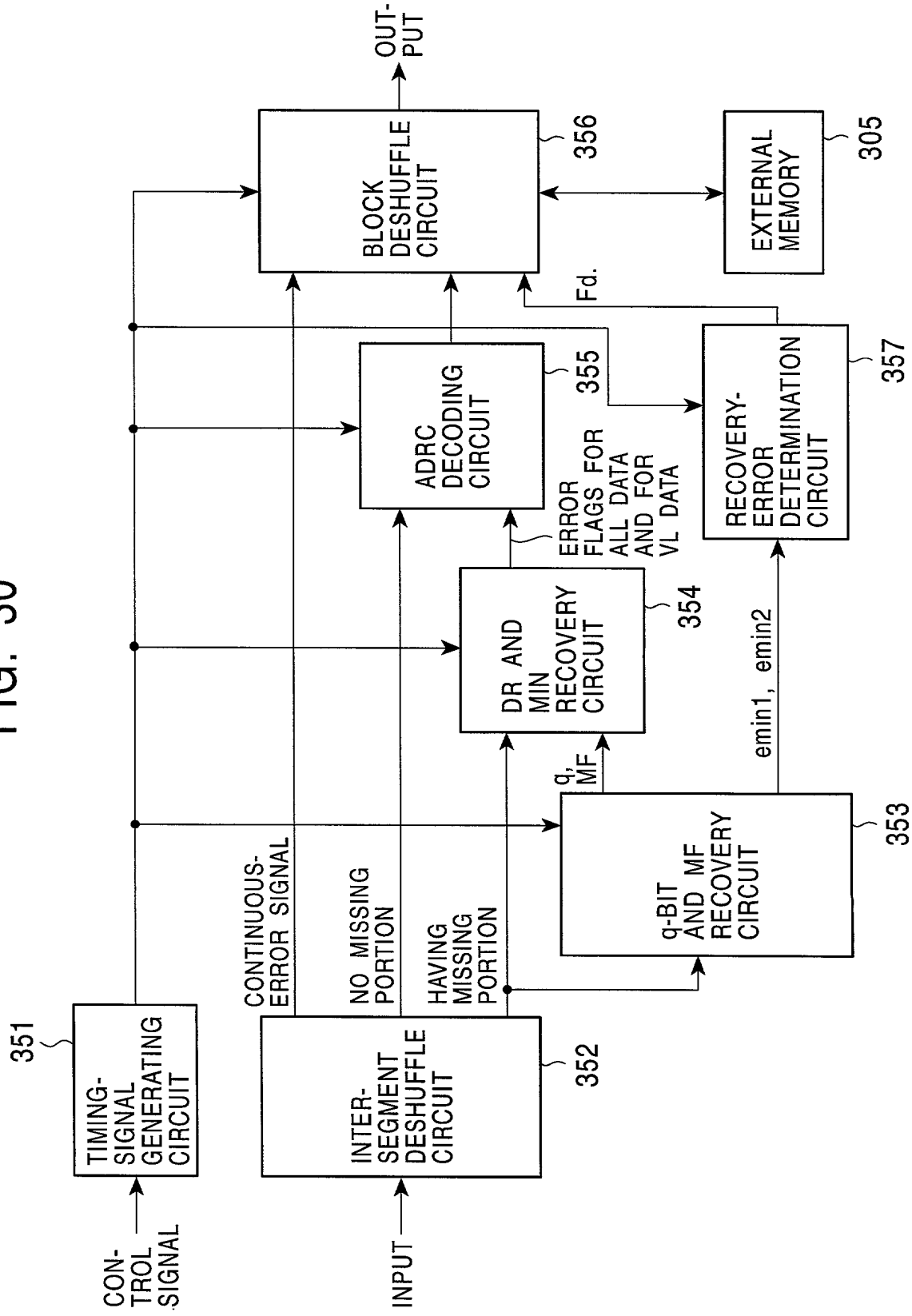

CON-
TROL
SIGNAL
INPUT
351
TIMING-
SIGNAL
GENERATING
CIRCUIT
352
INTER-
SEGMENT
DESHUFFLE
CIRCUIT
CONTINUOUS-
ERROR SIGNAL
NO MISSING
PORTION
HAVING
MISSING
PORTION
353
q-BIT
AND MF
RECOVERY
CIRCUIT
q,
MF
354
DR AND
MIN
RECOVERY
CIRCUIT
emin1, emin2
355
ADRC
DECODING
CIRCUIT
ERROR
FLAGS FOR
ALL DATA
AND FOR
VL DATA
357
RECOVERY-
ERROR
DETERMINATION
CIRCUIT
Fd.
356
BLOCK
DESHUFFLE
CIRCUIT
OUT-
PUT
305
EXTERNAL
MEMORY

FIG. 31

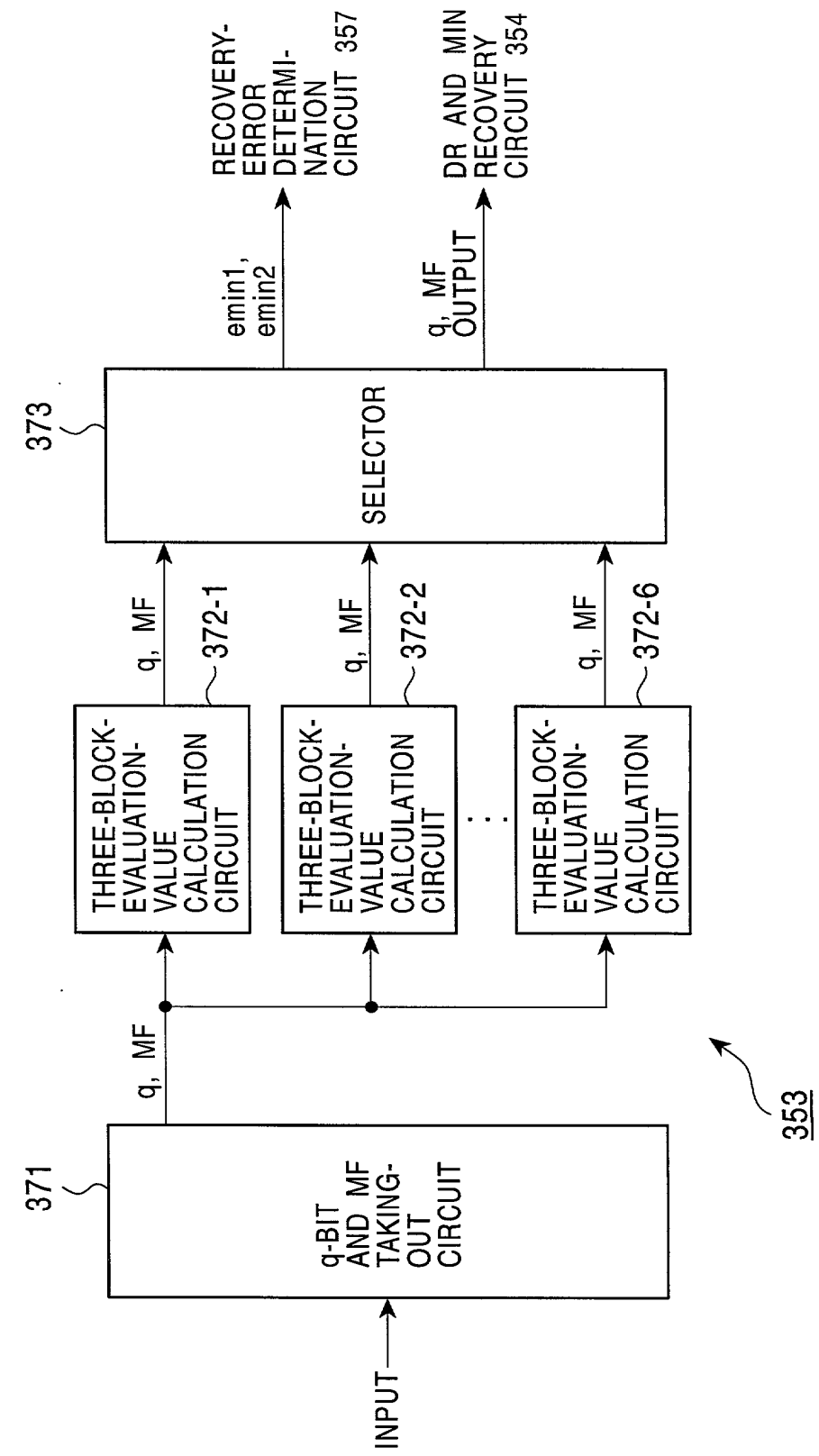

INPUT
371
q-BIT AND MF TAKING-OUT CIRCUIT
q, MF
THREE-BLOCK-EVALUATION-VALUE CALCULATION CIRCUIT
372-1
372-2
372-6
373
SELECTOR
emin1, emin2
RECOVERY-ERROR DETERMI-NATION CIRCUIT 357
q, MF OUTPUT
DR AND MIN RECOVERY CIRCUIT 354
353

FIG. 32

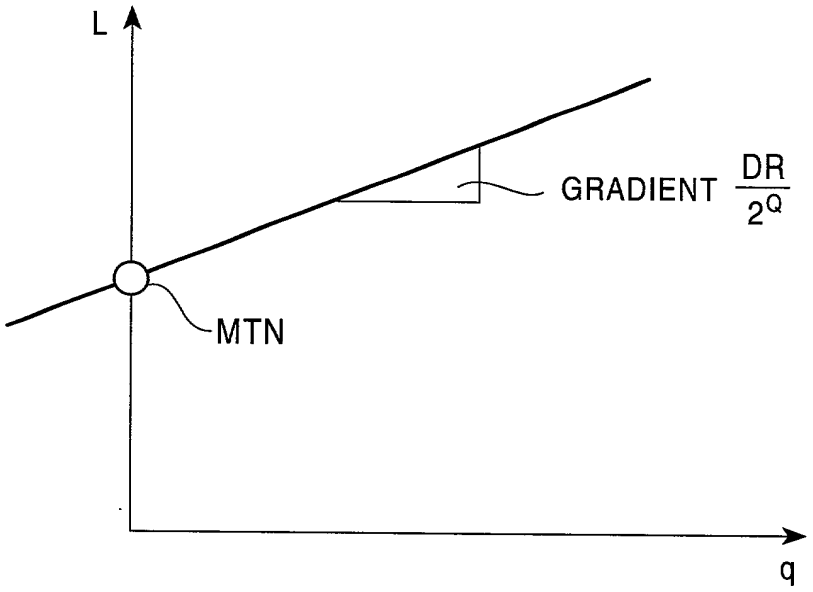


FIG. 33

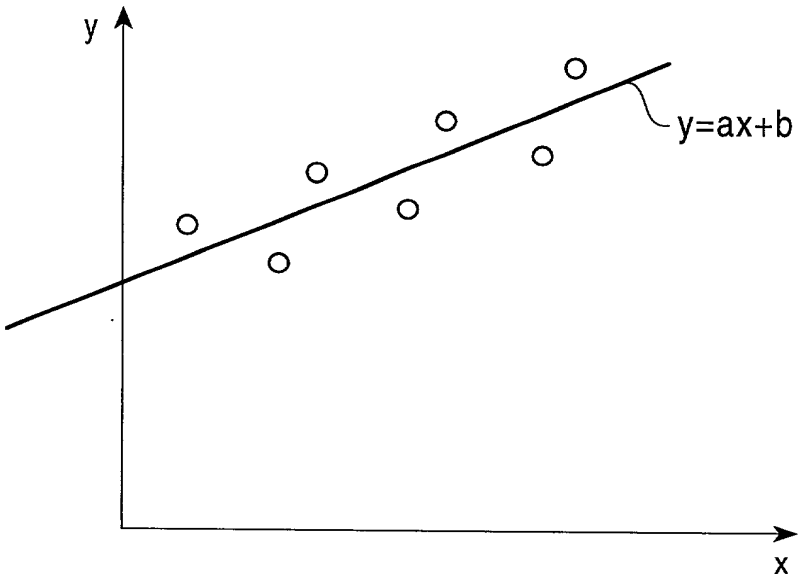


FIG. 34A

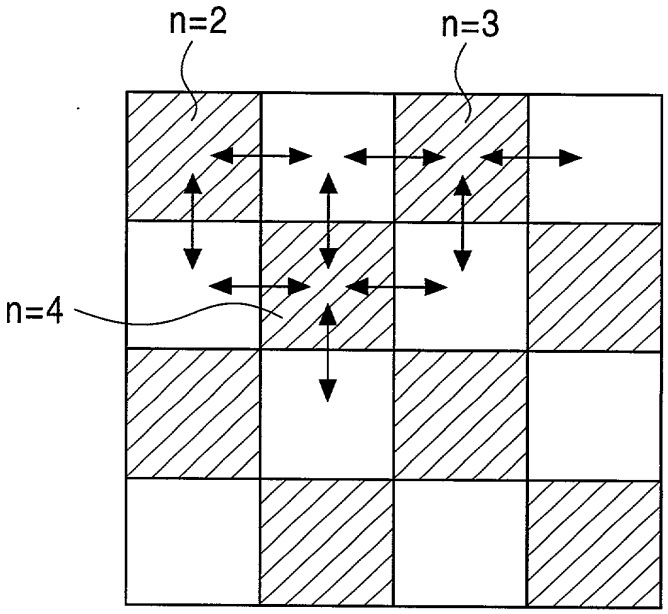


FIG. 34B

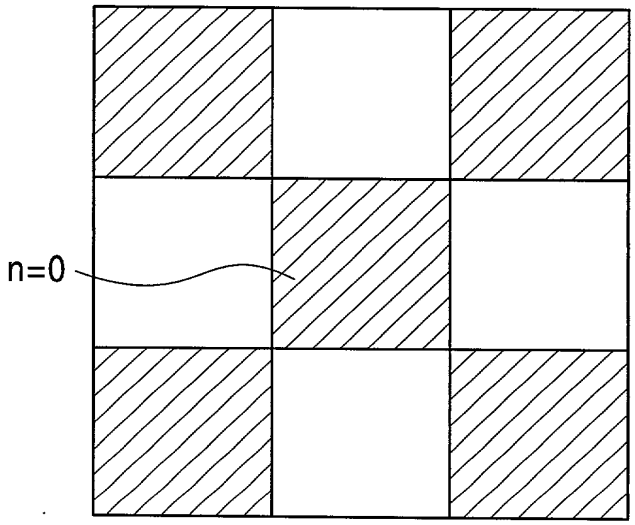


FIG. 35

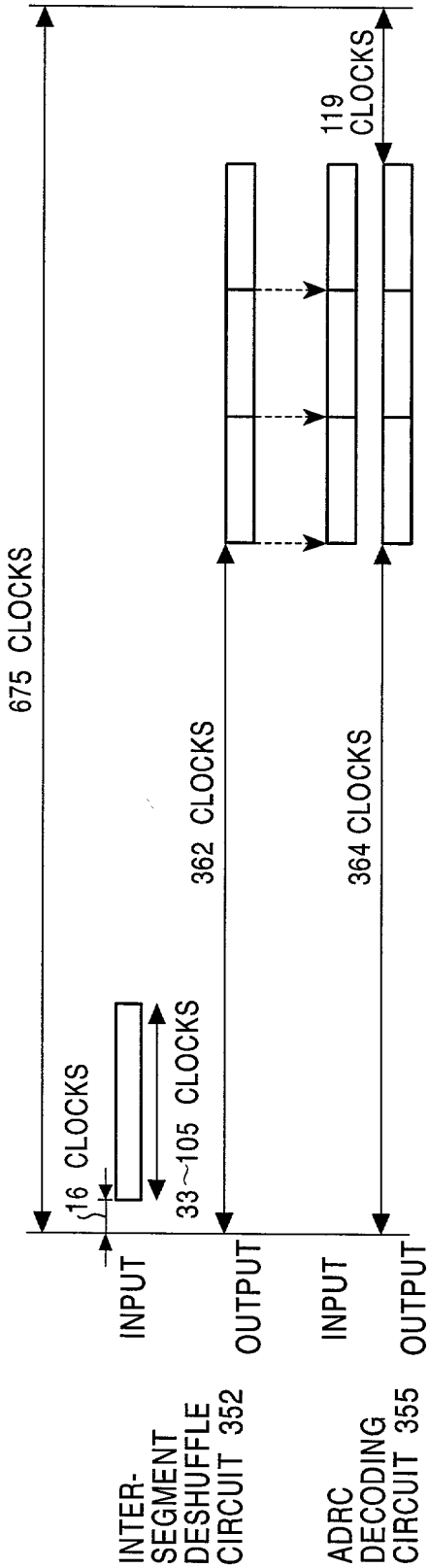

675 CLOCKS
16 CLOCKS
33~105 CLOCKS
362 CLOCKS
364 CLOCKS
119 CLOCKS
INPUT
OUTPUT
INPUT
OUTPUT
INTER-SEGMENT DESHUFFLE CIRCUIT 352
ADRC DECODING CIRCUIT 355

FIG. 36

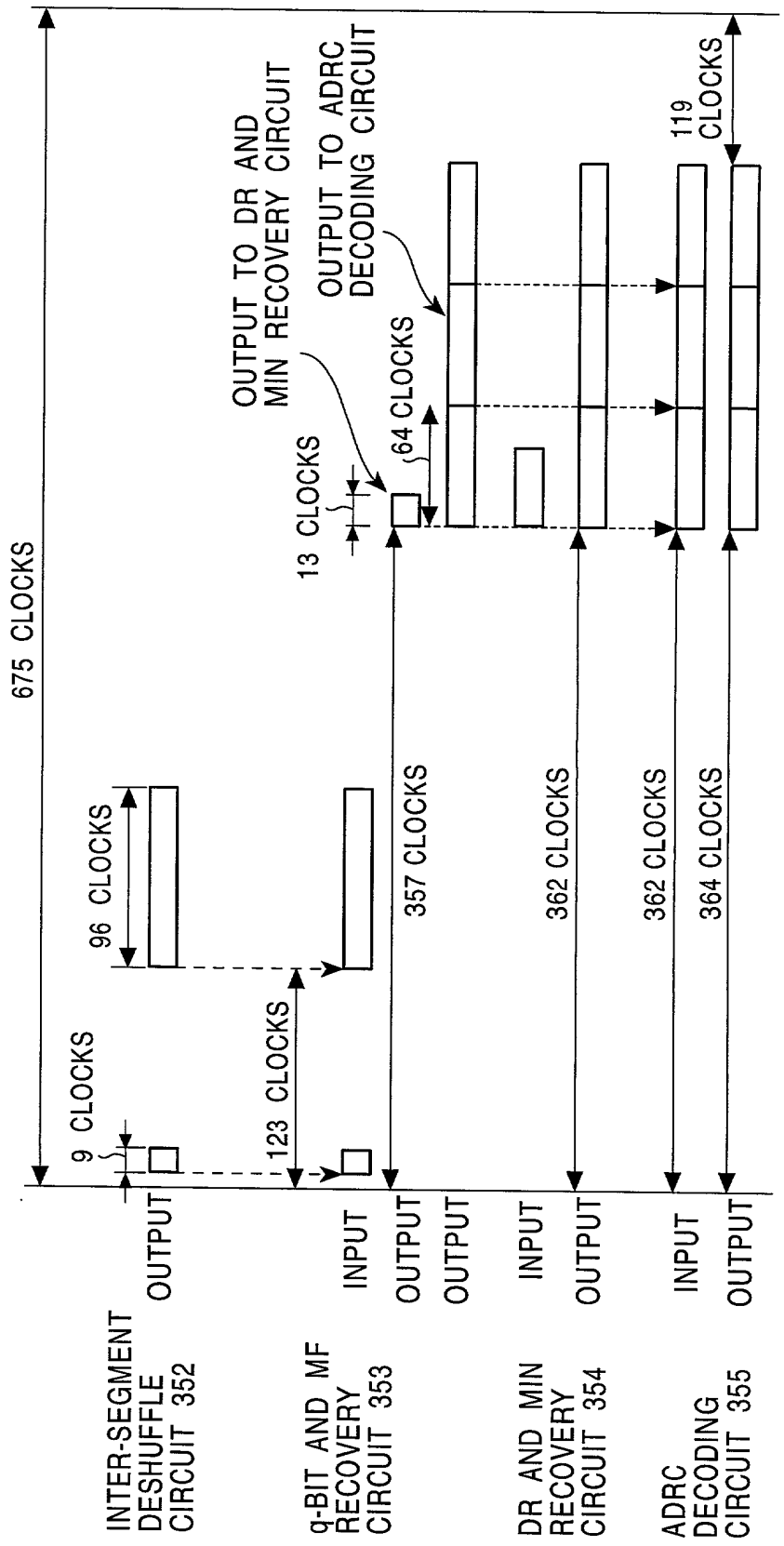

675 CLOCKS
9 CLOCKS
96 CLOCKS
123 CLOCKS
13 CLOCKS
64 CLOCKS
OUTPUT TO DR AND MIN RECOVERY CIRCUIT
OUTPUT TO ADRC DECODING CIRCUIT
357 CLOCKS
362 CLOCKS
362 CLOCKS
364 CLOCKS
119 CLOCKS
INTER-SEGMENT DESHUFFLE CIRCUIT 352
OUTPUT
q-BIT AND MF RECOVERY CIRCUIT 353
INPUT
OUTPUT
OUTPUT
DR AND MIN RECOVERY CIRCUIT 354
INPUT
OUTPUT
ADRC DECODING CIRCUIT 355
INPUT
OUTPUT

FIG. 37A

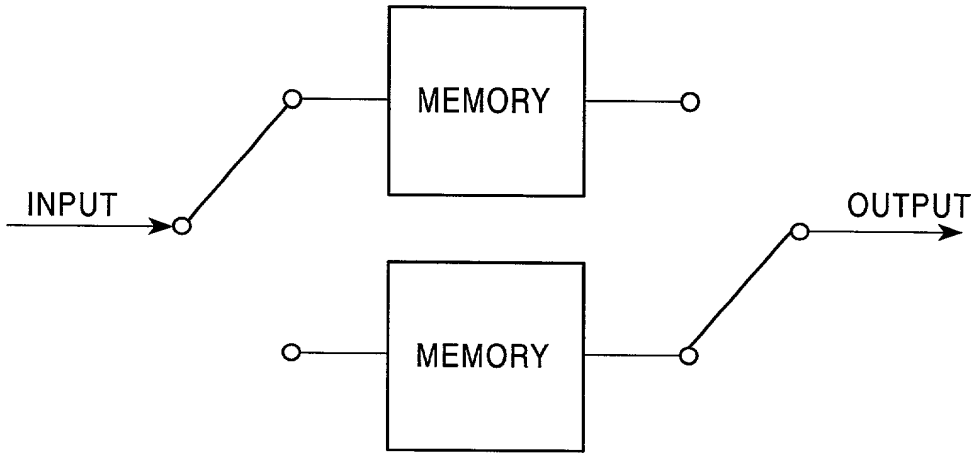


FIG. 37B

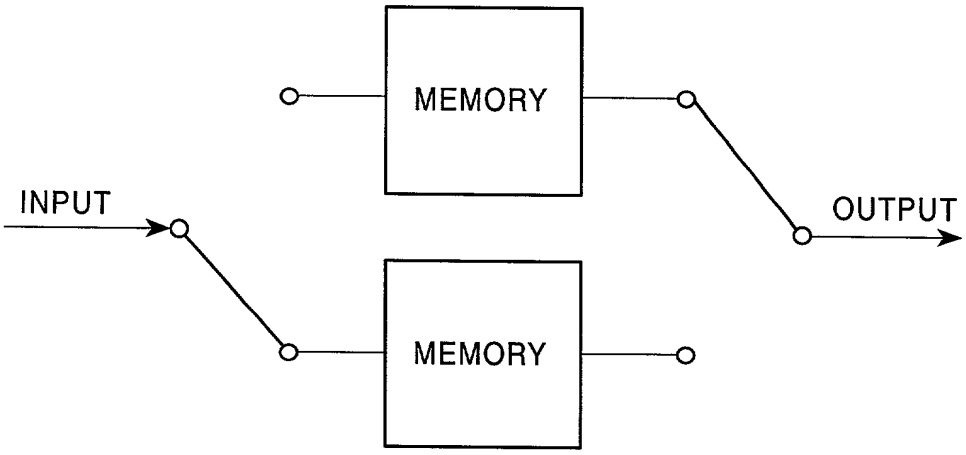


FIG. 38A

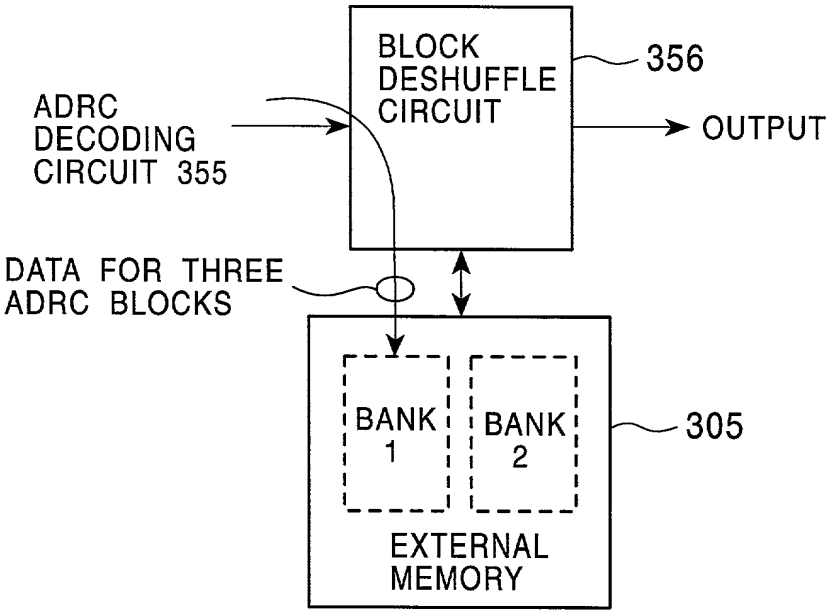


FIG. 38B

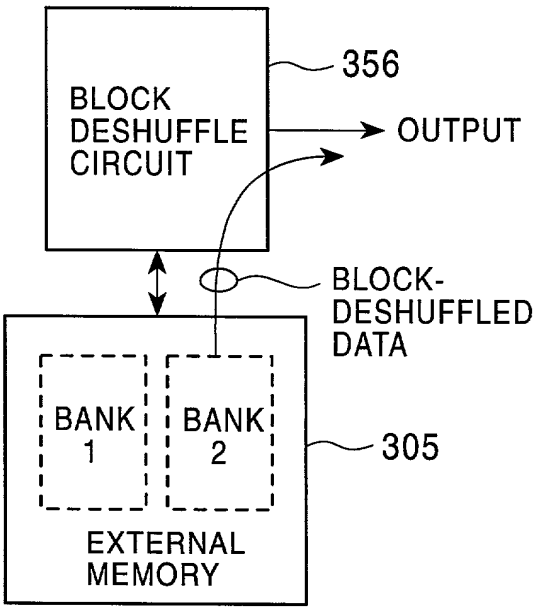


FIG. 39

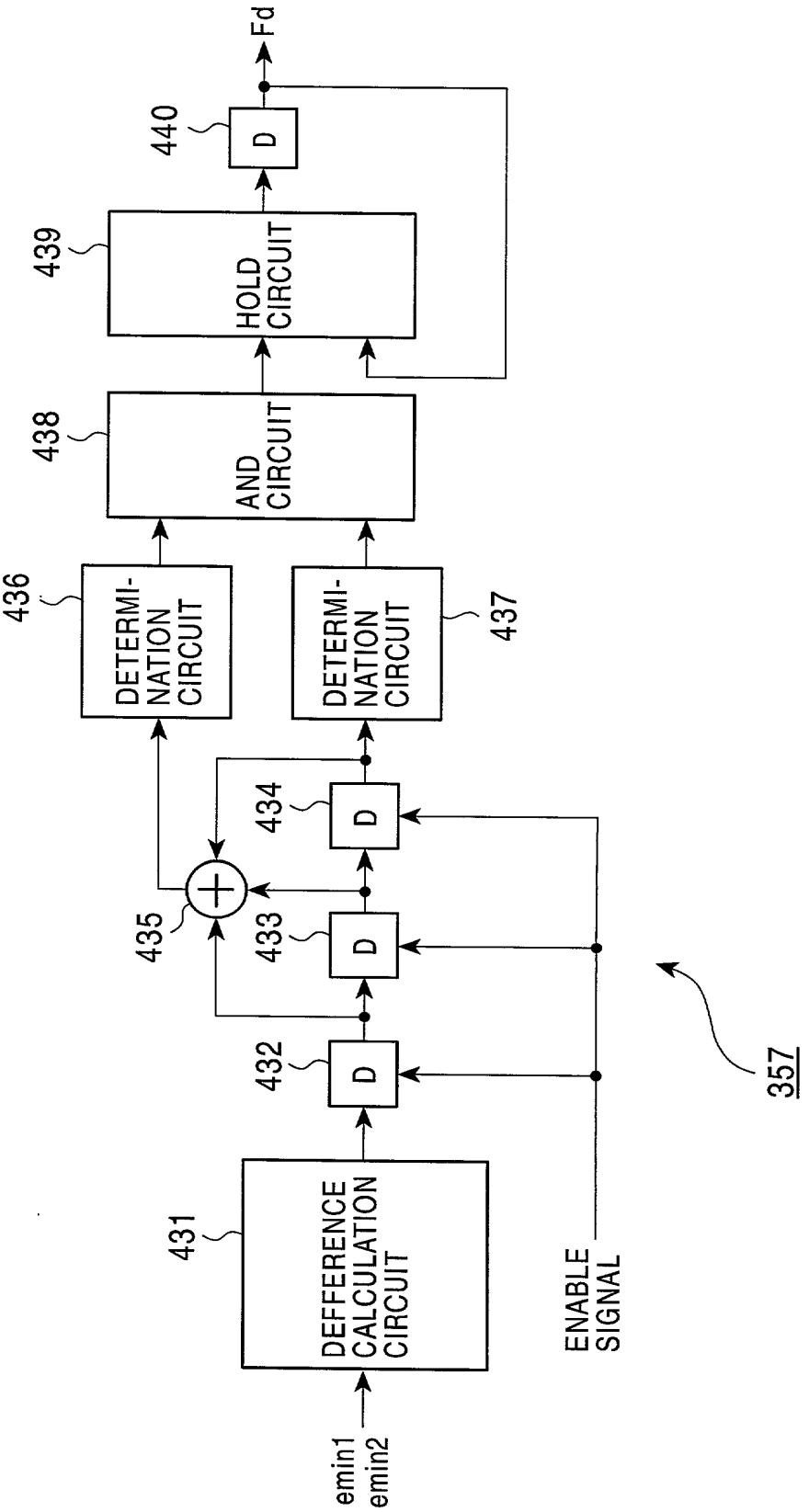

emin1
emin2
DEFFERENCE CALCULATION CIRCUIT
431
D
432
D
433
D
434
435
DETERMI-NATION CIRCUIT
436
DETERMI-NATION CIRCUIT
437
AND CIRCUIT
438
HOLD CIRCUIT
439
D
440
Fd
ENABLE SIGNAL
357

FIG. 40

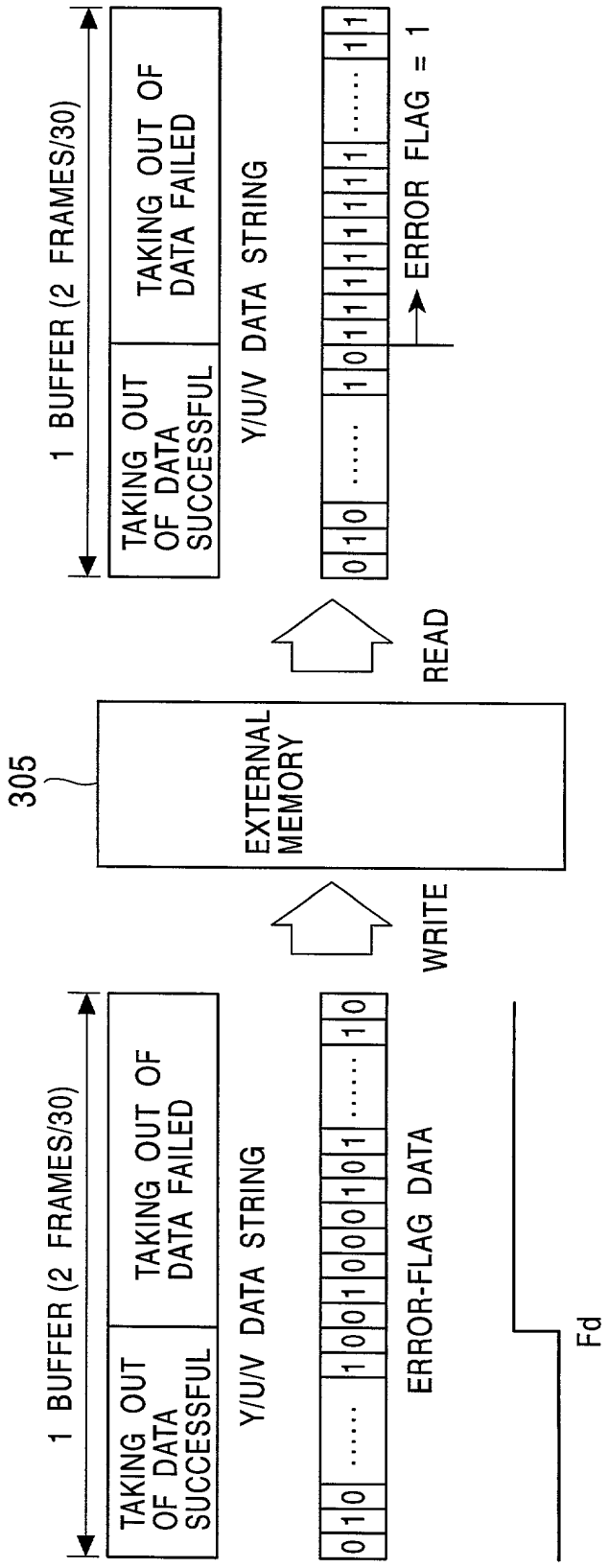

1 BUFFER (2 FRAMES/30)
TAKING OUT OF DATA SUCCESSFUL
TAKING OUT OF DATA FAILED
Y/U/V DATA STRING
0 1 0 ..... 1 0 0 1 0 0 0 1 0 1 ..... 1 0
ERROR-FLAG DATA
WRITE
305
EXTERNAL MEMORY
READ
0 1 0 ..... 1 0 1 1 1 1 1 1 1 1 ..... 1 1
ERROR FLAG = 1
Fd

FIG. 41

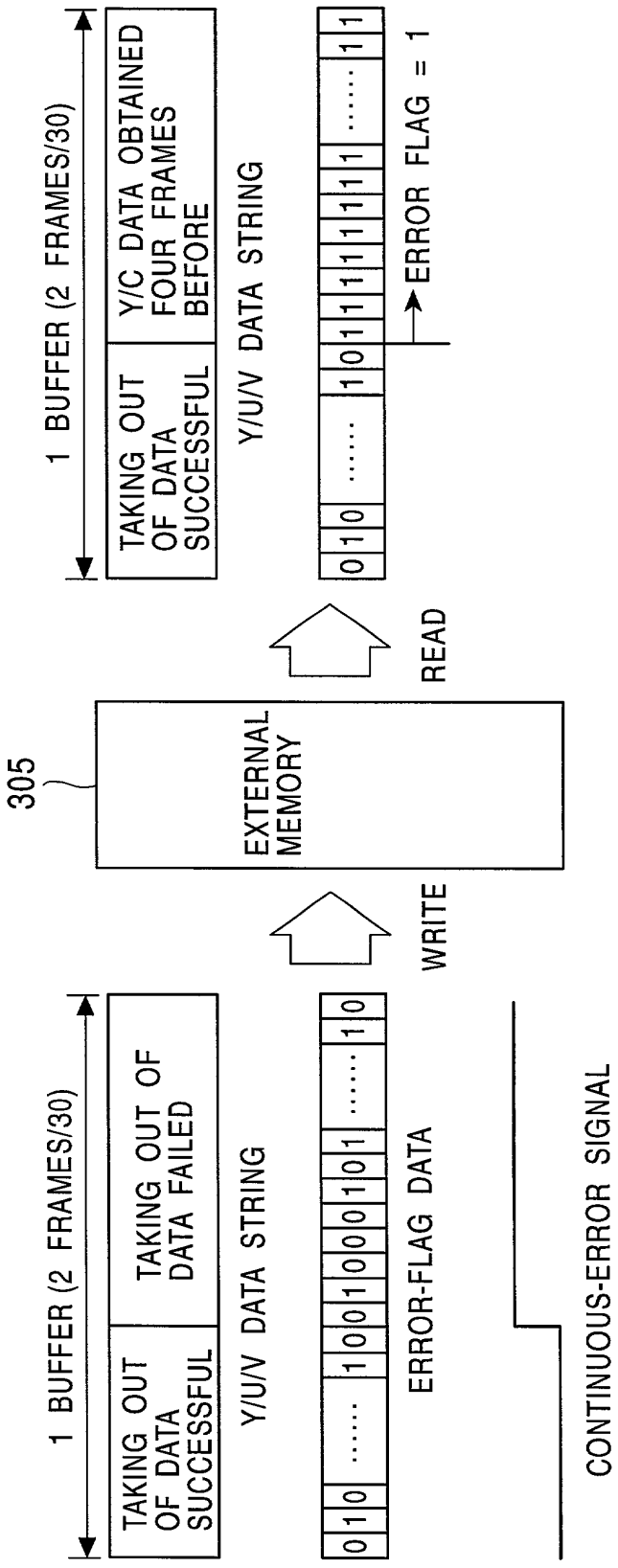

1 BUFFER (2 FRAMES/30)
TAKING OUT OF DATA SUCCESSFUL
TAKING OUT OF DATA FAILED
Y/U/V DATA STRING
0 1 0 ..... 1 0 0 1 0 0 0 1 0 1 ..... 1 0
ERROR-FLAG DATA
WRITE
305
EXTERNAL MEMORY
READ
1 BUFFER (2 FRAMES/30)
TAKING OUT OF DATA SUCCESSFUL
Y/C DATA OBTAINED FOUR FRAMES BEFORE
Y/U/V DATA STRING
0 1 0 ..... 1 0 1 1 1 1 1 1 1 1 ..... 1 1
ERROR FLAG = 1
CONTINUOUS-ERROR SIGNAL

FIG. 42

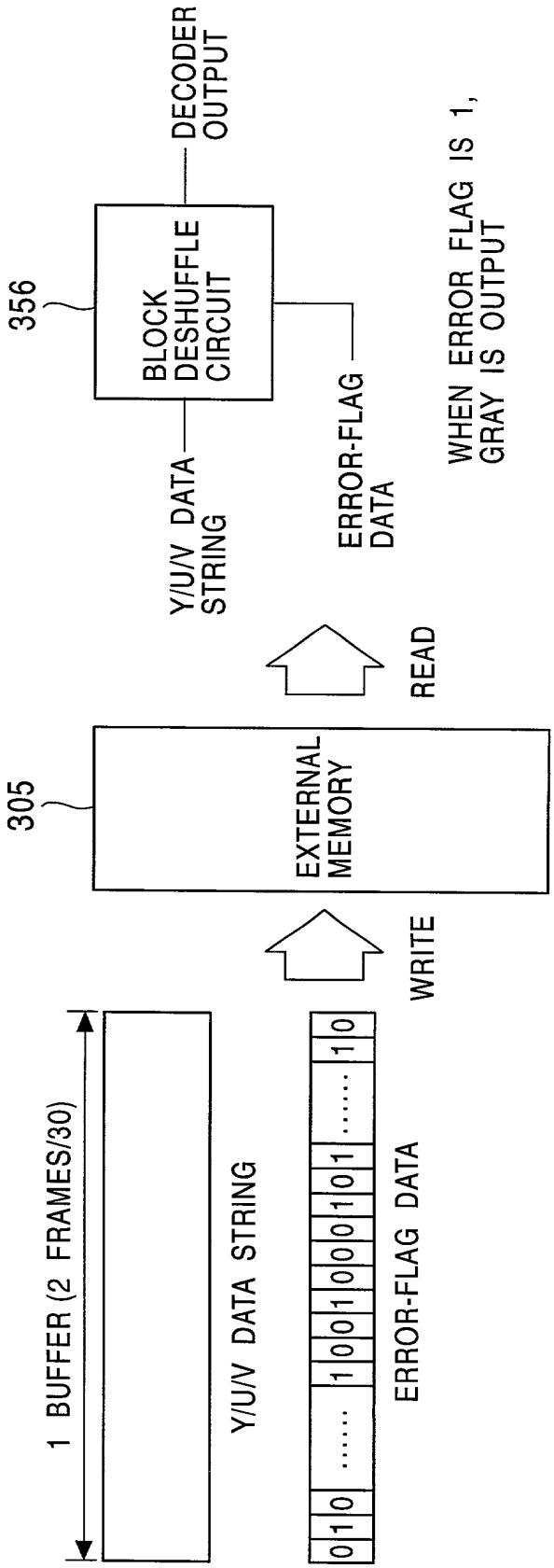

1 BUFFER (2 FRAMES/30)
Y/U/V DATA STRING
ERROR-FLAG DATA
0 1 0 ..... 1 0 0 1 0 0 0 1 0 1 1 ..... 1 0
WRITE
305
EXTERNAL MEMORY
READ
Y/U/V DATA STRING
ERROR-FLAG DATA
356
BLOCK DESHUFFLE CIRCUIT
DECODER OUTPUT
WHEN ERROR FLAG IS 1, GRAY IS OUTPUT

FIG. 43

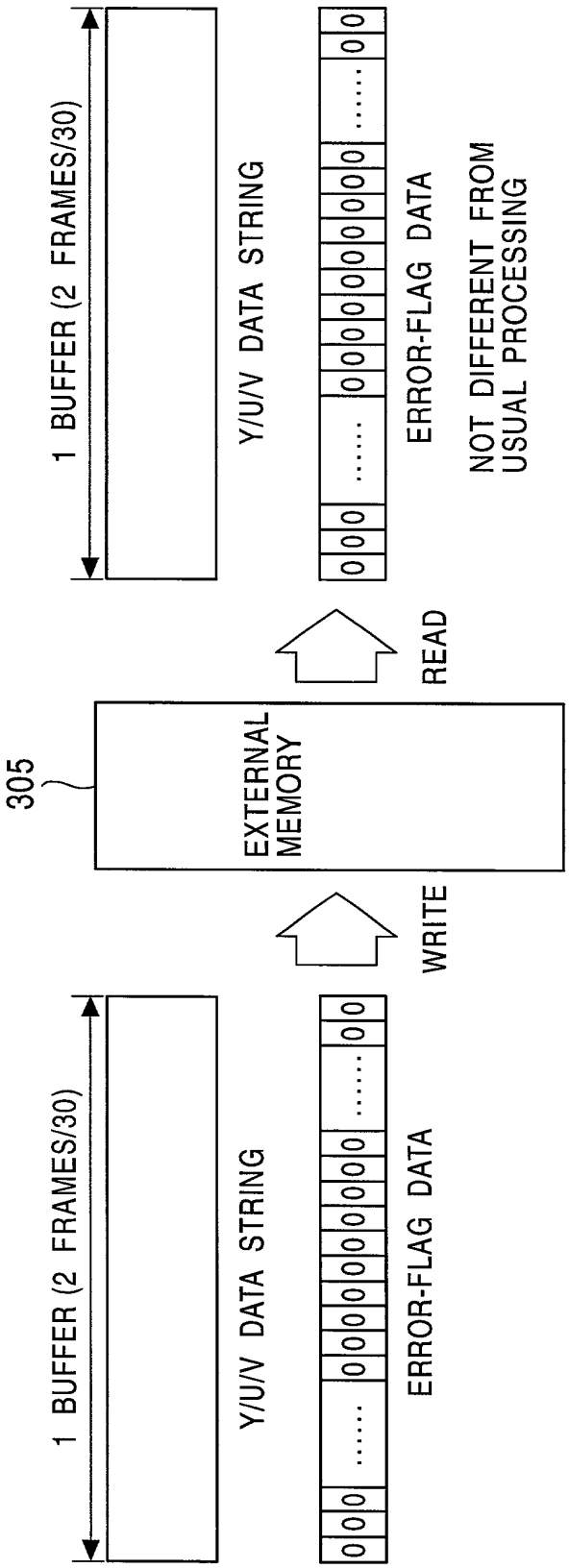

1 BUFFER (2 FRAMES/30)
Y/U/V DATA STRING
ERROR-FLAG DATA
0 0 0 ..... 0 0 0 0 0 0 0 0 ..... 0 0
WRITE
305
EXTERNAL MEMORY
READ
1 BUFFER (2 FRAMES/30)
Y/U/V DATA STRING
ERROR-FLAG DATA
0 0 0 ..... 0 0 0 0 0 0 0 0 ..... 0 0
NOT DIFFERENT FROM USUAL PROCESSING

FIG. 44

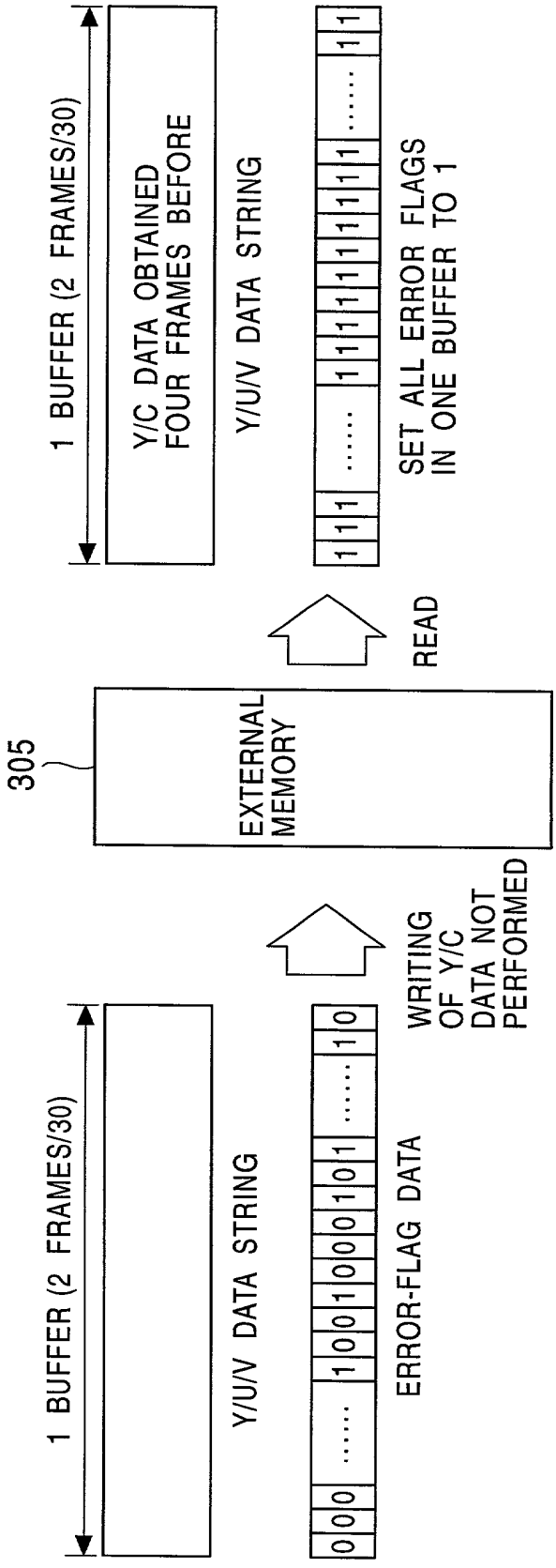

1 BUFFER (2 FRAMES/30)
Y/C DATA OBTAINED FOUR FRAMES BEFORE
Y/U/V DATA STRING
1 1 1 ..... 1 1 1 1 1 1 1 1 1 1 1 ..... 1 1
SET ALL ERROR FLAGS IN ONE BUFFER TO 1
READ
305
EXTERNAL MEMORY
WRITING OF Y/C DATA NOT PERFORMED
0 0 0 ..... 1 0 0 1 0 0 0 1 0 1 ..... 1 0
ERROR-FLAG DATA
Y/U/V DATA STRING
1 BUFFER (2 FRAMES/30)

FIG. 45

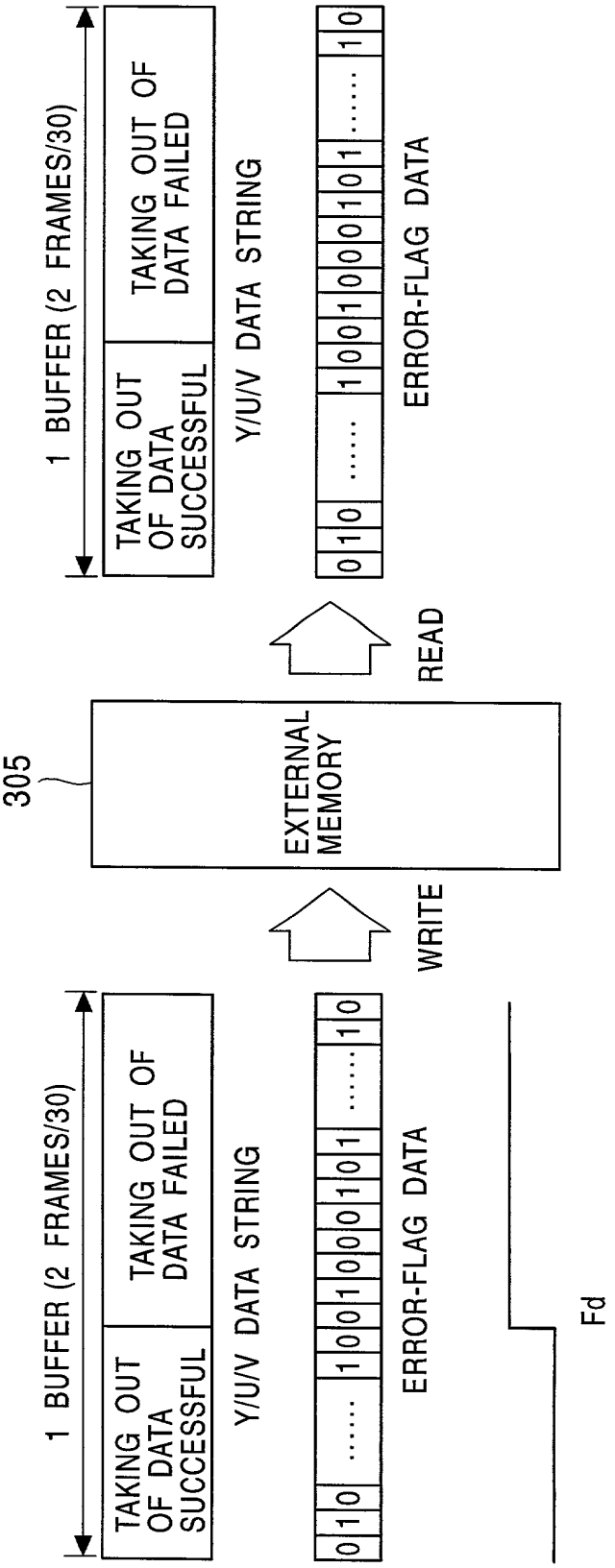

1 BUFFER (2 FRAMES/30)
TAKING OUT OF DATA SUCCESSFUL
TAKING OUT OF DATA FAILED
Y/U/V DATA STRING
ERROR-FLAG DATA
0 1 0 ..... 1 0 0 1 0 0 0 1 0 1 ..... 1 0
305
EXTERNAL MEMORY
WRITE
READ
Fd

FIG. 46

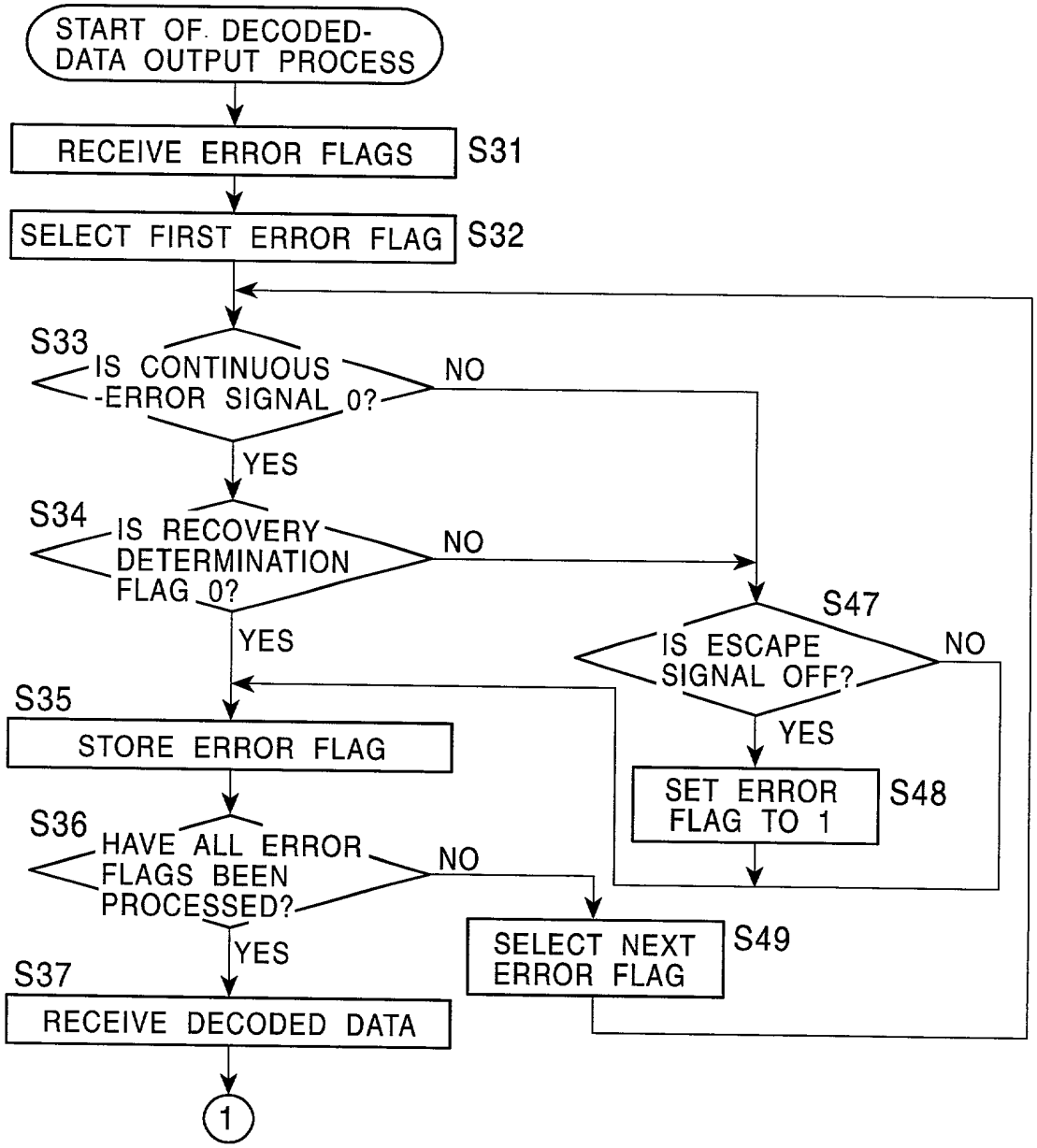

START OF DECODED-DATA OUTPUT PROCESS
RECEIVE ERROR FLAGS
S31
SELECT FIRST ERROR FLAG
S32
S33
IS CONTINUOUS -ERROR SIGNAL 0?
NO
YES
S34
IS RECOVERY DETERMINATION FLAG 0?
NO
YES
S47
IS ESCAPE SIGNAL OFF?
NO
YES
S35
STORE ERROR FLAG
SET ERROR FLAG TO 1
S48
S36
HAVE ALL ERROR FLAGS BEEN PROCESSED?
NO
YES
SELECT NEXT ERROR FLAG
S49
S37
RECEIVE DECODED DATA
1

FIG. 47

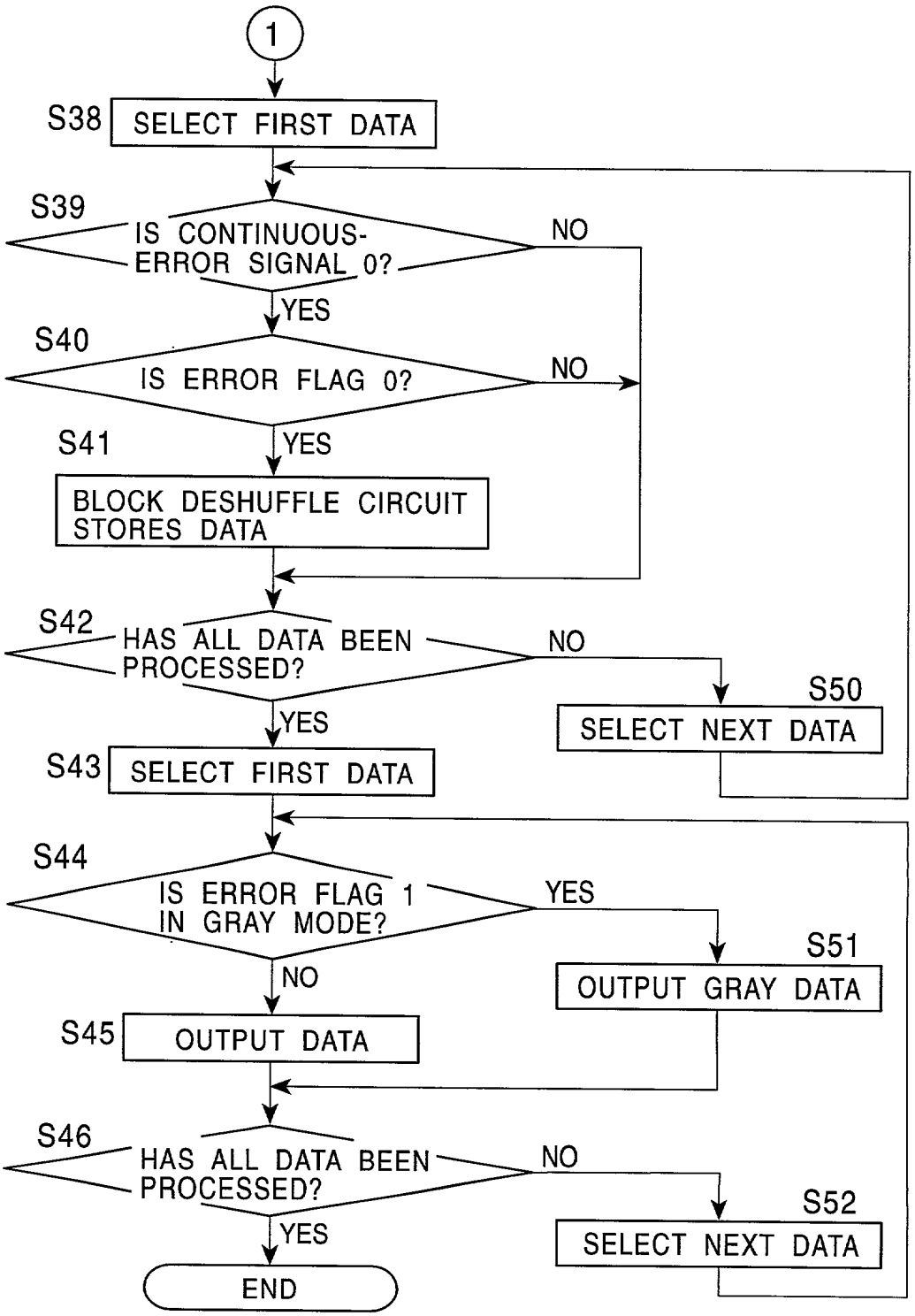

1
S38
SELECT FIRST DATA
S39
IS CONTINUOUS-ERROR SIGNAL 0?
NO
YES
S40
IS ERROR FLAG 0?
NO
YES
S41
BLOCK DESHUFFLE CIRCUIT STORES DATA
S42
HAS ALL DATA BEEN PROCESSED?
NO
YES
S50
SELECT NEXT DATA
S43
SELECT FIRST DATA
S44
IS ERROR FLAG 1 IN GRAY MODE?
YES
NO
S51
OUTPUT GRAY DATA
S45
OUTPUT DATA
S46
HAS ALL DATA BEEN PROCESSED?
NO
YES
S52
SELECT NEXT DATA
END

FIG. 48

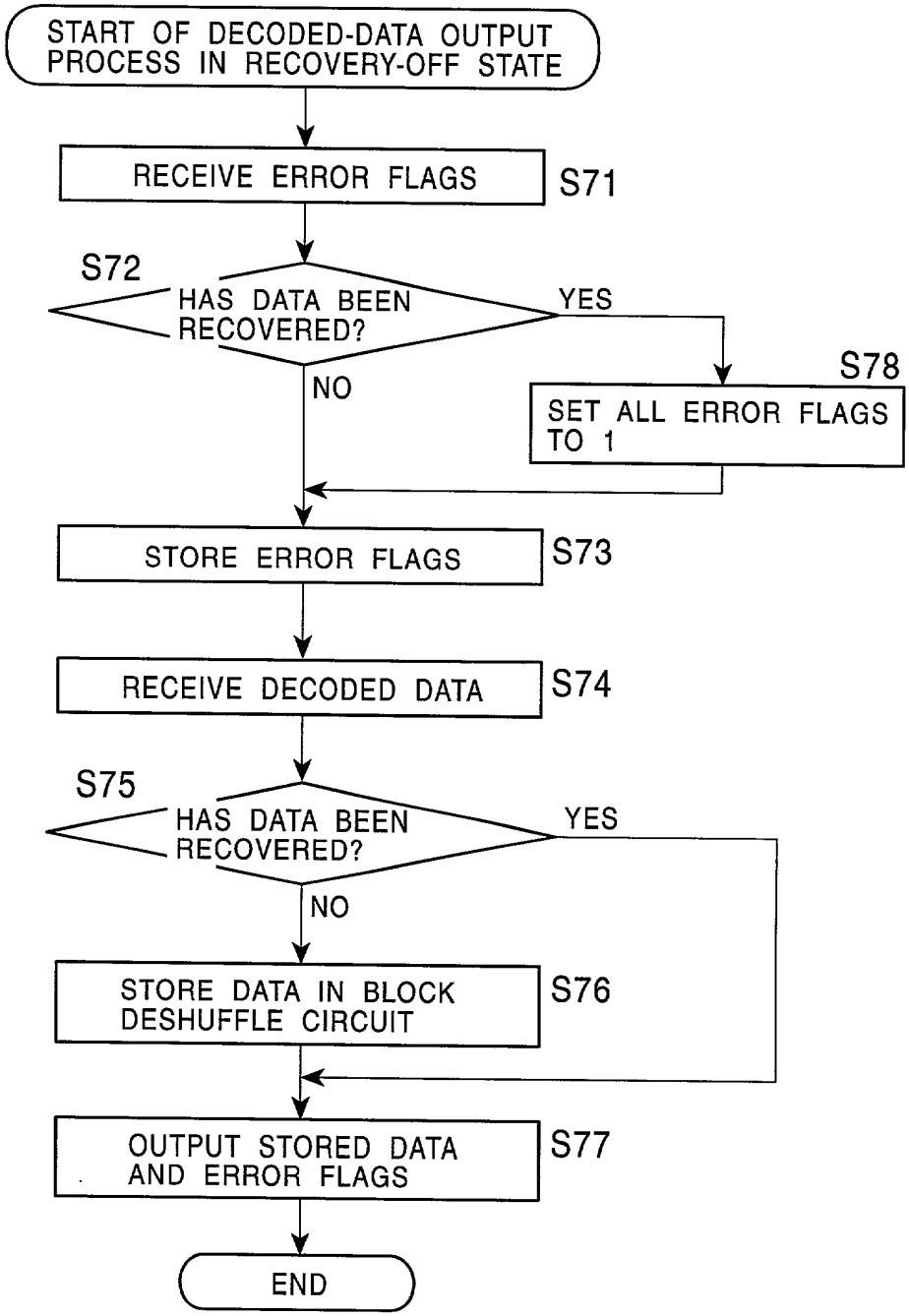

START OF DECODED-DATA OUTPUT PROCESS IN RECOVERY-OFF STATE
RECEIVE ERROR FLAGS
S71
S72
HAS DATA BEEN RECOVERED?
YES
NO
S78
SET ALL ERROR FLAGS TO 1
STORE ERROR FLAGS
S73
RECEIVE DECODED DATA
S74
S75
HAS DATA BEEN RECOVERED?
YES
NO
STORE DATA IN BLOCK DESHUFFLE CIRCUIT
S76
OUTPUT STORED DATA AND ERROR FLAGS
S77
END

FIG. 49A

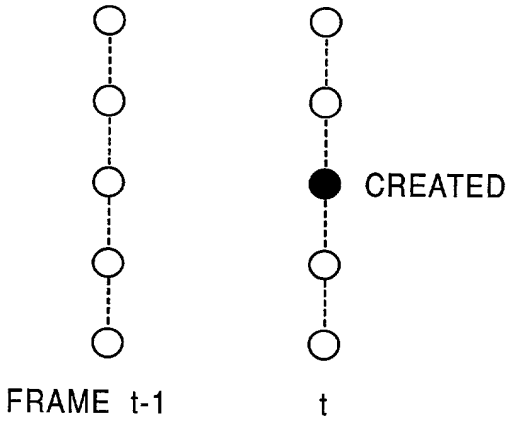


FIG. 49B

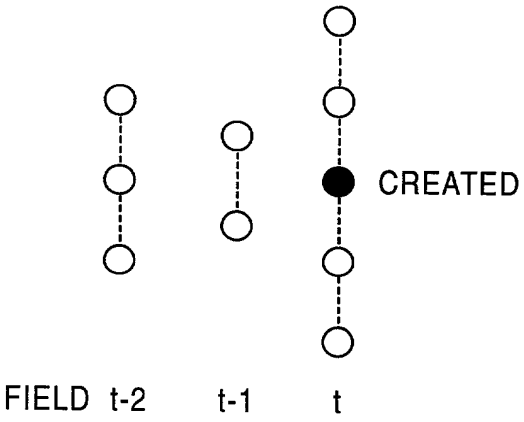


FIG. 50

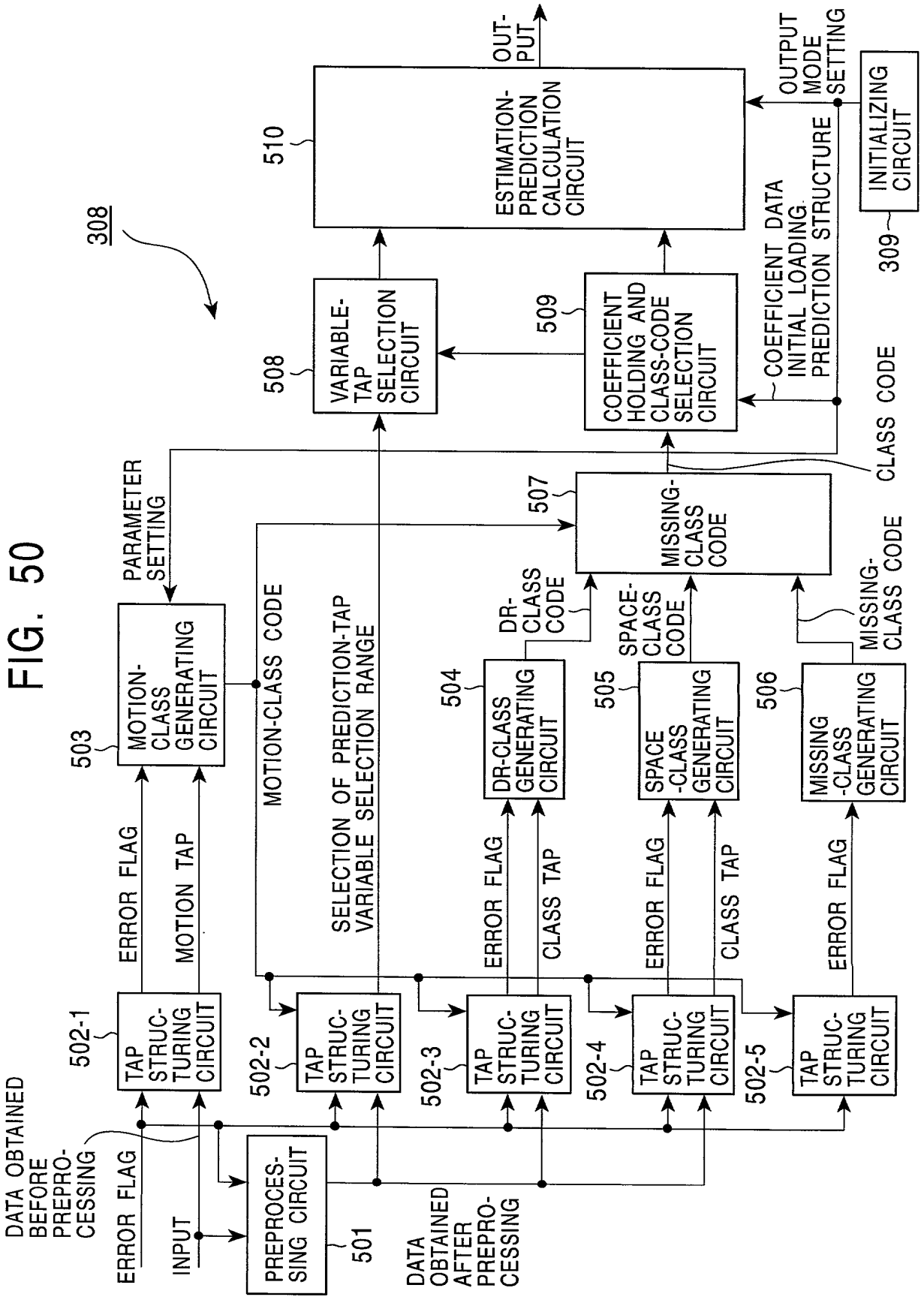

DATA OBTAINED BEFORE PREPRO-CESSING
ERROR FLAG
INPUT
PREPROCES-SING CIRCUIT
501
DATA OBTAINED AFTER PREPRO-CESSING
502-1
TAP STRUC-TURING CIRCUIT
502-2
TAP STRUC-TURING CIRCUIT
502-3
TAP STRUC-TURING CIRCUIT
502-4
TAP STRUC-TURING CIRCUIT
502-5
TAP STRUC-TURING CIRCUIT
ERROR FLAG
MOTION TAP
ERROR FLAG
CLASS TAP
ERROR FLAG
CLASS TAP
ERROR FLAG
503
MOTION-CLASS GENERATING CIRCUIT
PARAMETER SETTING
MOTION-CLASS CODE
SELECTION OF PREDICTION-TAP VARIABLE SELECTION RANGE
504
DR-CLASS GENERATING CIRCUIT
DR-CLASS CODE
505
SPACE-CLASS GENERATING CIRCUIT
SPACE-CLASS CODE
506
MISSING-CLASS GENERATING CIRCUIT
MISSING-CLASS CODE
507
MISSING-CLASS CODE
CLASS CODE
308
508
VARIABLE-TAP SELECTION CIRCUIT
509
COEFFICIENT HOLDING AND CLASS-CODE SELECTION CIRCUIT
COEFFICIENT DATA INITIAL LOADING PREDICTION STRUCTURE
510
ESTIMATION-PREDICTION CALCULATION CIRCUIT
OUT-PUT
OUTPUT MODE SETTING
309
INITIALIZING CIRCUIT

FIG. 51

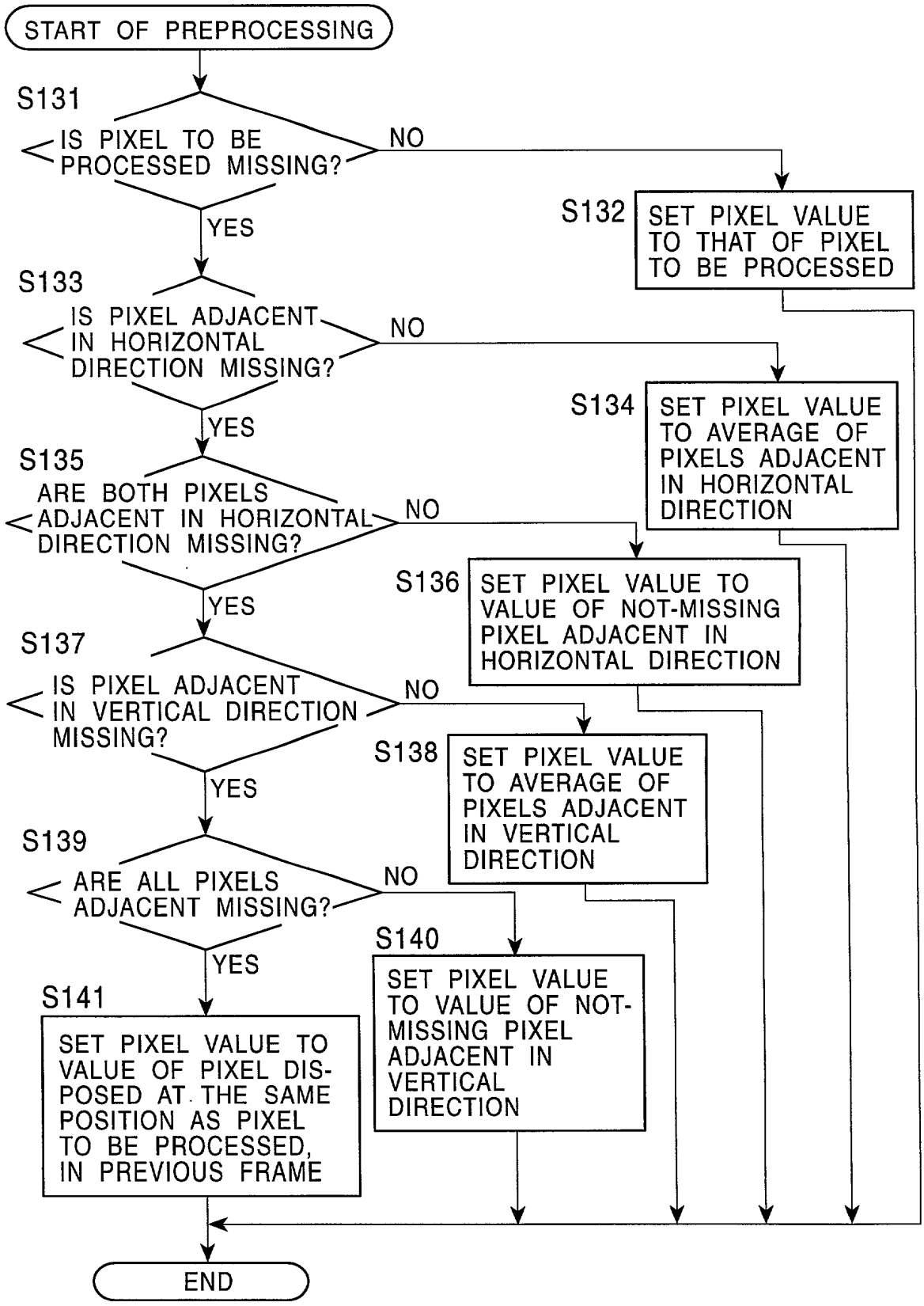

START OF PREPROCESSING
S131
IS PIXEL TO BE PROCESSED MISSING?
NO
YES
S132
SET PIXEL VALUE TO THAT OF PIXEL TO BE PROCESSED
S133
IS PIXEL ADJACENT IN HORIZONTAL DIRECTION MISSING?
NO
YES
S134
SET PIXEL VALUE TO AVERAGE OF PIXELS ADJACENT IN HORIZONTAL DIRECTION
S135
ARE BOTH PIXELS ADJACENT IN HORIZONTAL DIRECTION MISSING?
NO
YES
S136
SET PIXEL VALUE TO VALUE OF NOT-MISSING PIXEL ADJACENT IN HORIZONTAL DIRECTION
S137
IS PIXEL ADJACENT IN VERTICAL DIRECTION MISSING?
NO
YES
S138
SET PIXEL VALUE TO AVERAGE OF PIXELS ADJACENT IN VERTICAL DIRECTION
S139
ARE ALL PIXELS ADJACENT MISSING?
NO
YES
S140
SET PIXEL VALUE TO VALUE OF NOT-MISSING PIXEL ADJACENT IN VERTICAL DIRECTION
S141
SET PIXEL VALUE TO VALUE OF PIXEL DISPOSED AT THE SAME POSITION AS PIXEL TO BE PROCESSED, IN PREVIOUS FRAME
END

FIG. 52A

	H1	H2	H3
L1	ERROR	q2	q3
L2	q4	ERROR	q6
L3	q7	ERROR	q9

FRAME t

FIG. 52B

	H1	H2	H3
L1	p1	p2	p3
L2	p4	p5	p6
L3	p7	p8	p9

FRAME t-1

FIG. 53

q1	q2	q3
q4	ERROR	q6
q7	q8	q9

FRAME t

FIG. 54

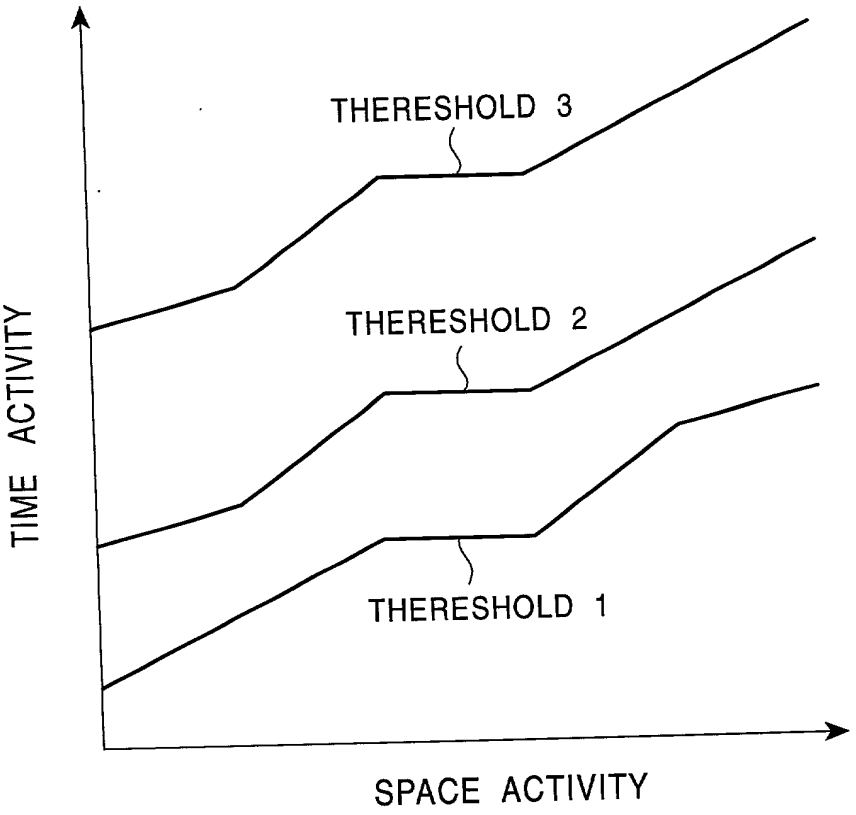

THERESHOLD 3
THERESHOLD 2
THERESHOLD 1
TIME ACTIVITY
SPACE ACTIVITY

FIG. 55

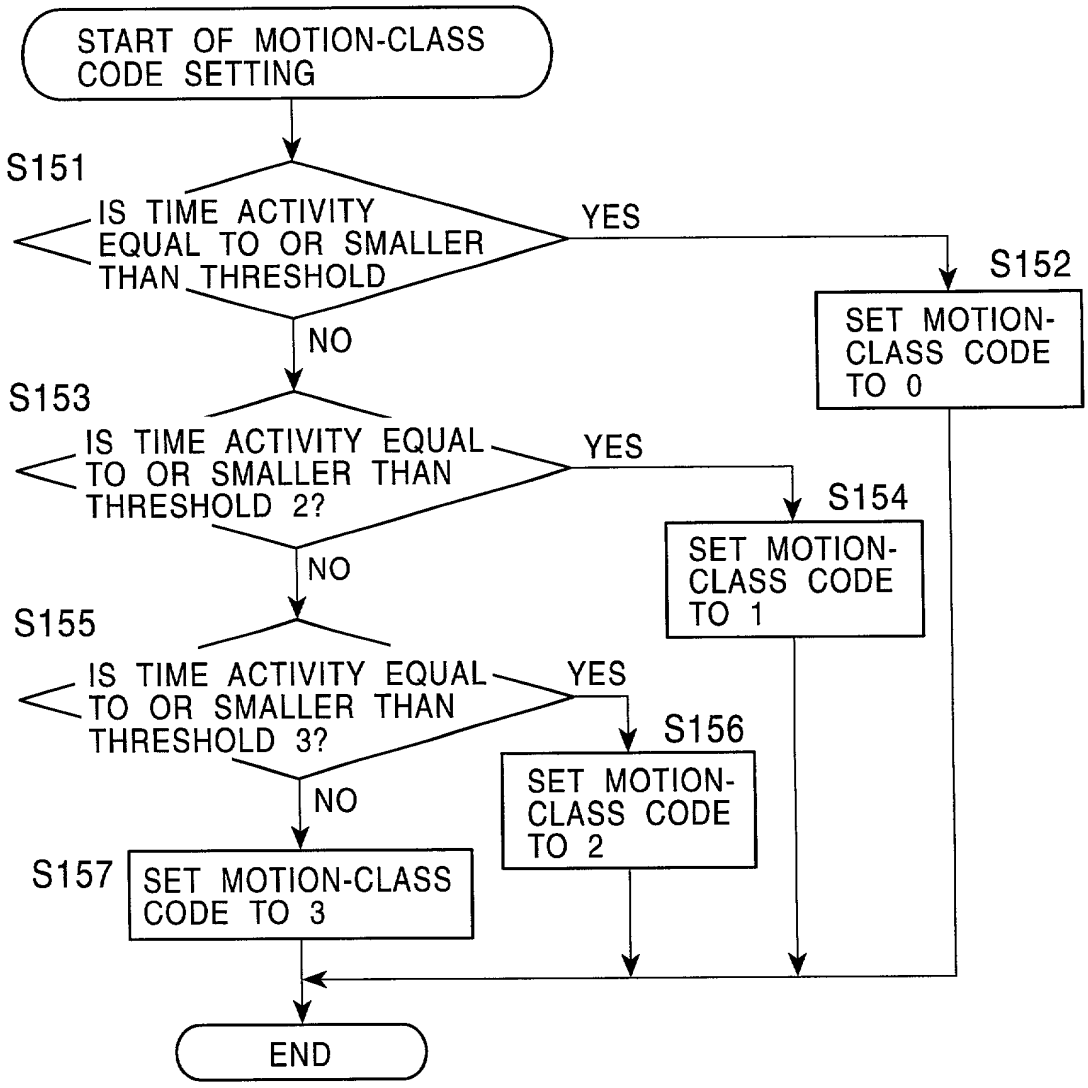
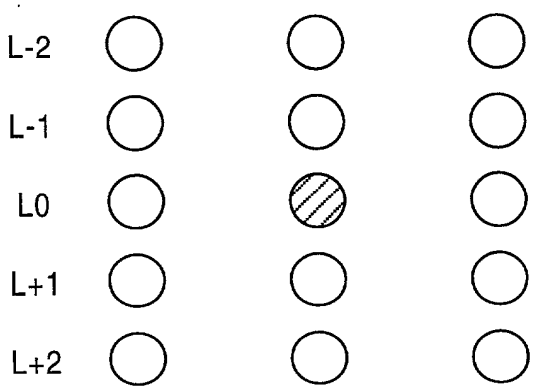

START OF MOTION-CLASS CODE SETTING
S151
IS TIME ACTIVITY EQUAL TO OR SMALLER THAN THRESHOLD
YES
S152
SET MOTION-CLASS CODE TO 0
NO
S153
IS TIME ACTIVITY EQUAL TO OR SMALLER THAN THRESHOLD 2?
YES
S154
SET MOTION-CLASS CODE TO 1
NO
S155
IS TIME ACTIVITY EQUAL TO OR SMALLER THAN THRESHOLD 3?
YES
S156
SET MOTION-CLASS CODE TO 2
NO
S157
SET MOTION-CLASS CODE TO 3
END

FIG. 56



: PIXEL TO BE PROCESSED

FIG. 57

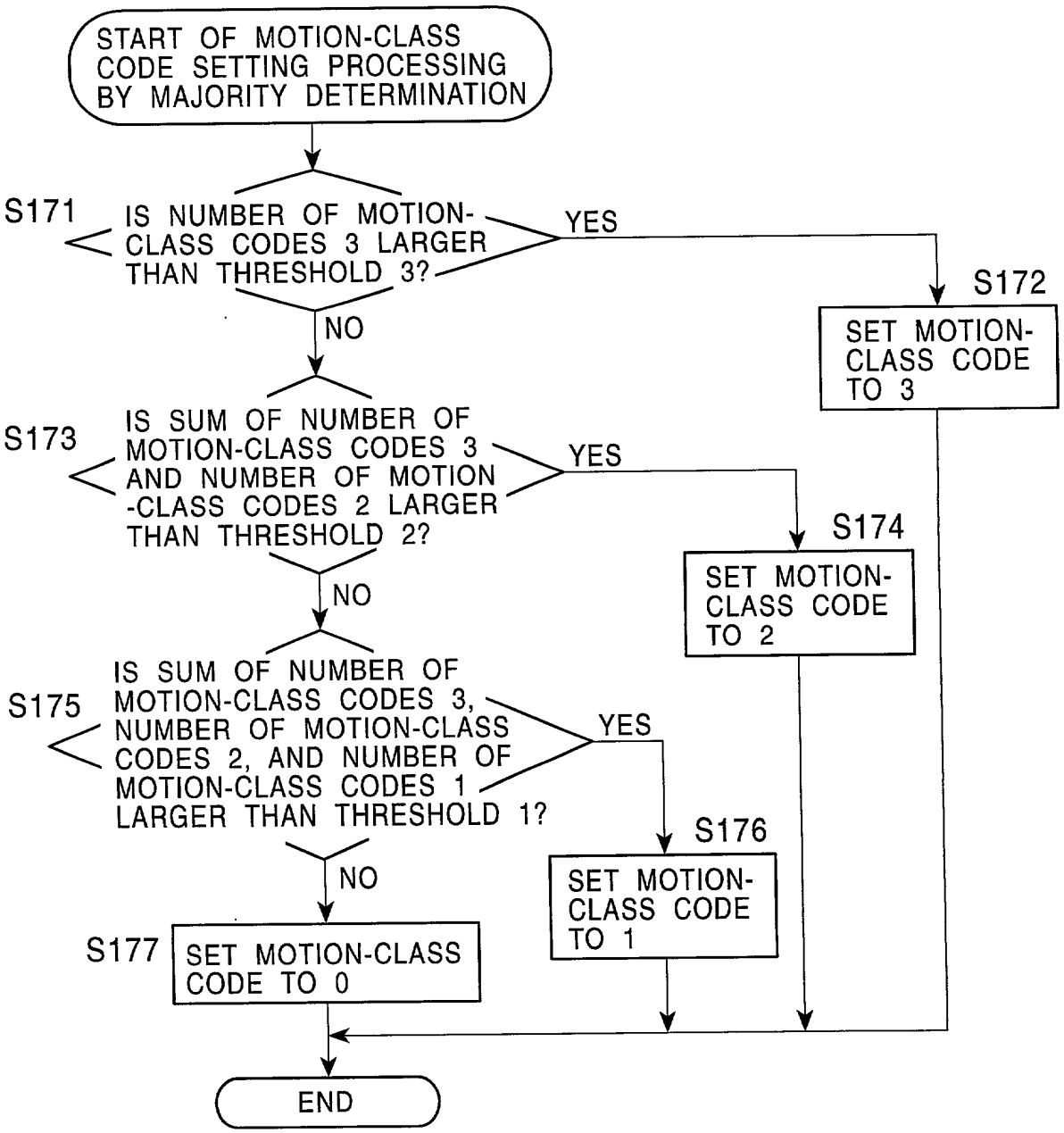

START OF MOTION-CLASS CODE SETTING PROCESSING BY MAJORITY DETERMINATION
S171
IS NUMBER OF MOTION-CLASS CODES 3 LARGER THAN THRESHOLD 3?
YES
NO
S172
SET MOTION-CLASS CODE TO 3
S173
IS SUM OF NUMBER OF MOTION-CLASS CODES 3 AND NUMBER OF MOTION-CLASS CODES 2 LARGER THAN THRESHOLD 2?
YES
NO
S174
SET MOTION-CLASS CODE TO 2
S175
IS SUM OF NUMBER OF MOTION-CLASS CODES 3, NUMBER OF MOTION-CLASS CODES 2, AND NUMBER OF MOTION-CLASS CODES 1 LARGER THAN THRESHOLD 1?
YES
NO
S176
SET MOTION-CLASS CODE TO 1
S177
SET MOTION-CLASS CODE TO 0
END

FIG. 58

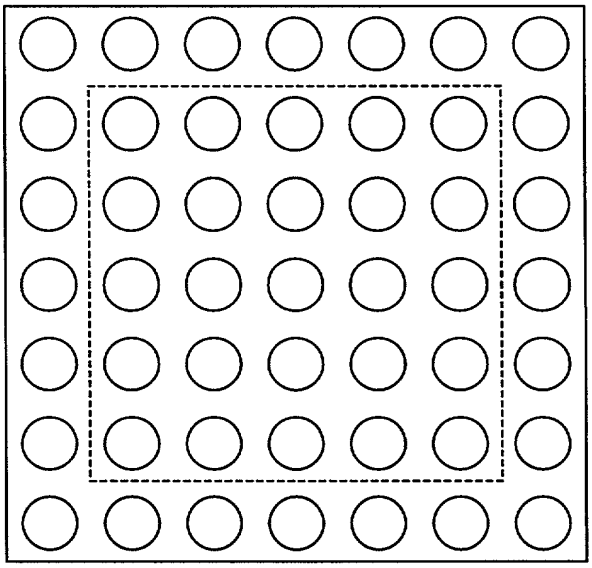


FIG. 59

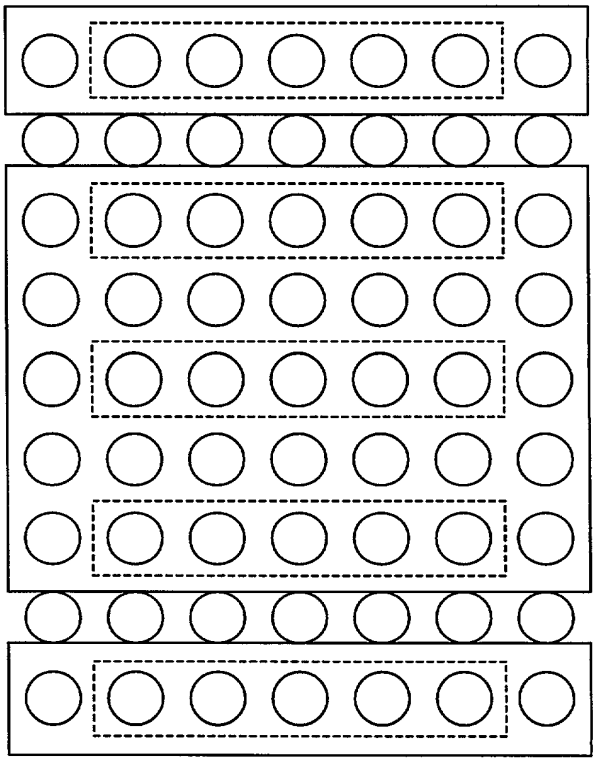


FIG. 60

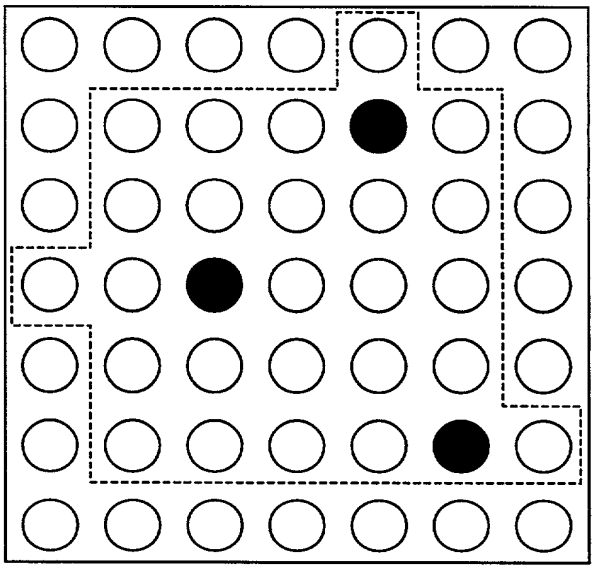


FIG. 61

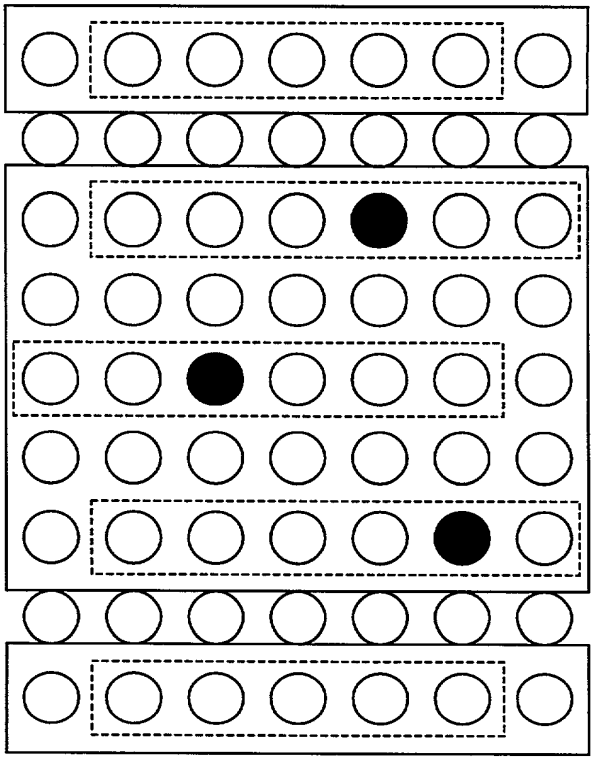


FIG. 62A

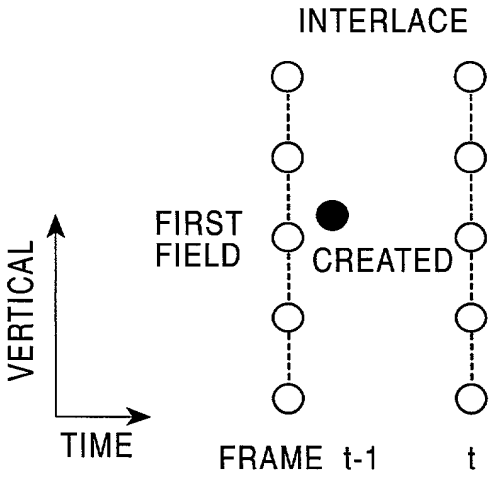


FIG. 62C

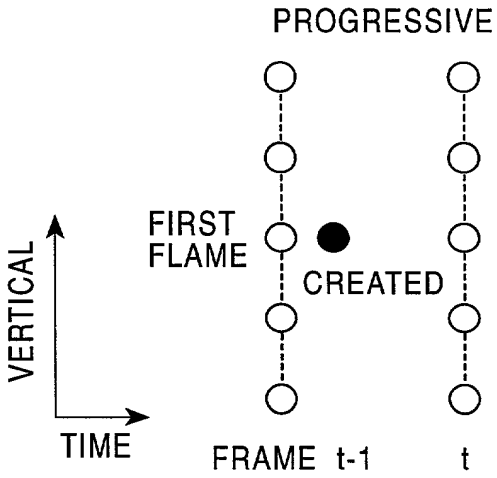


FIG. 62B

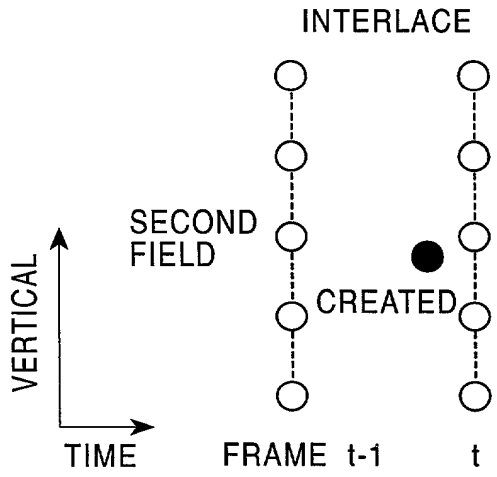


FIG. 62D

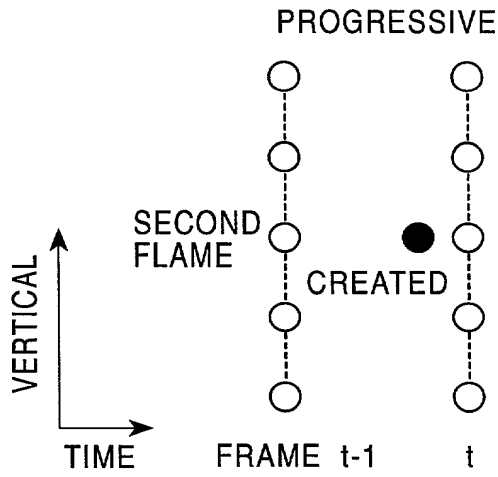


FIG. 63

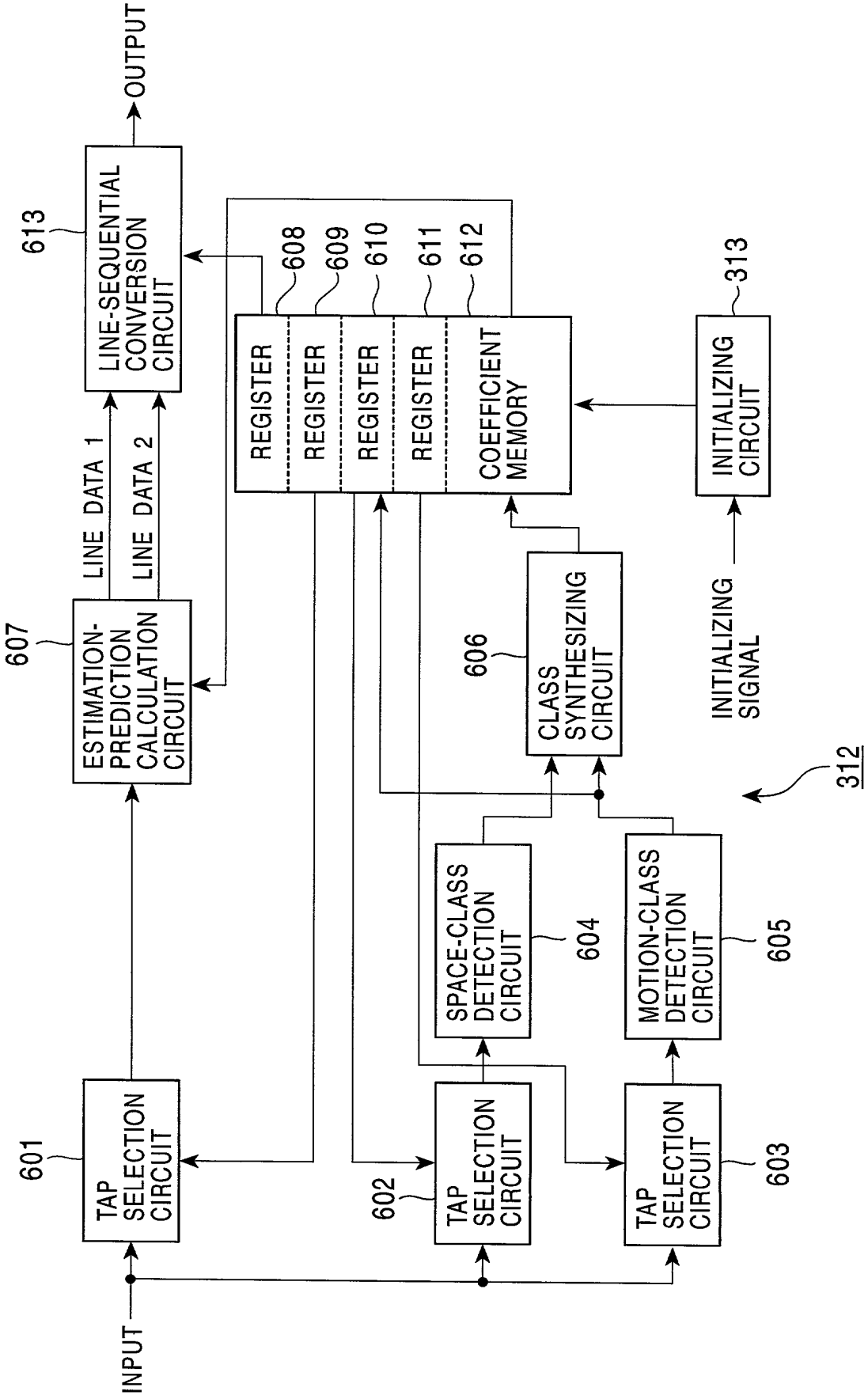

INPUT
TAP SELECTION CIRCUIT
601
TAP SELECTION CIRCUIT
602
TAP SELECTION CIRCUIT
603
SPACE-CLASS DETECTION CIRCUIT
604
MOTION-CLASS DETECTION CIRCUIT
605
CLASS SYNTHESIZING CIRCUIT
606
312
INITIALIZING SIGNAL
INITIALIZING CIRCUIT
313
ESTIMATION-PREDICTION CALCULATION CIRCUIT
607
LINE DATA 1
LINE DATA 2
REGISTER
608
REGISTER
609
REGISTER
610
REGISTER
611
COEFFICIENT MEMORY
612
LINE-SEQUENTIAL CONVERSION CIRCUIT
613
OUTPUT

FIG. 64

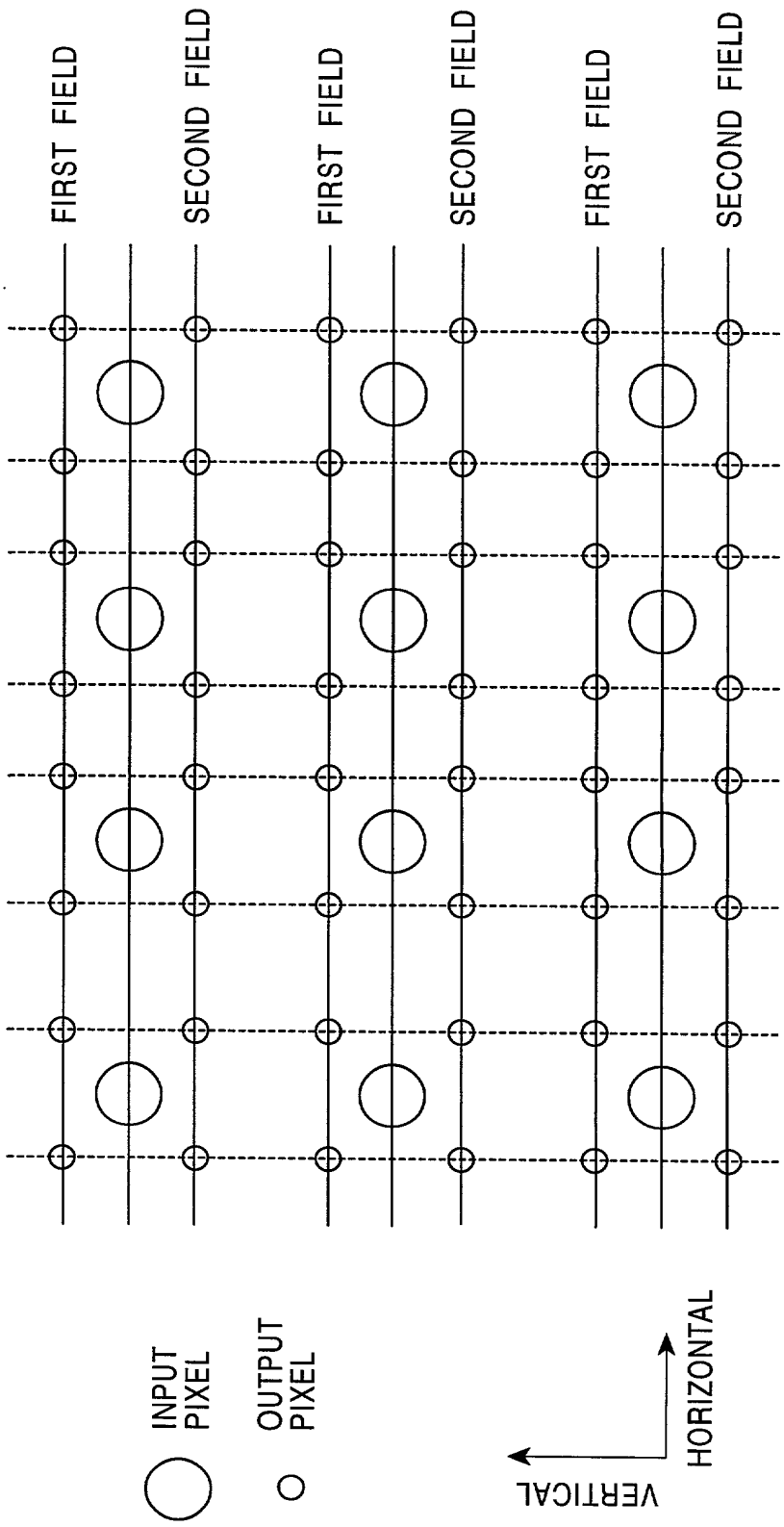

FIRST FIELD
SECOND FIELD
FIRST FIELD
SECOND FIELD
FIRST FIELD
SECOND FIELD
INPUT PIXEL
OUTPUT PIXEL
VERTICAL
HORIZONTAL

FIG. 65

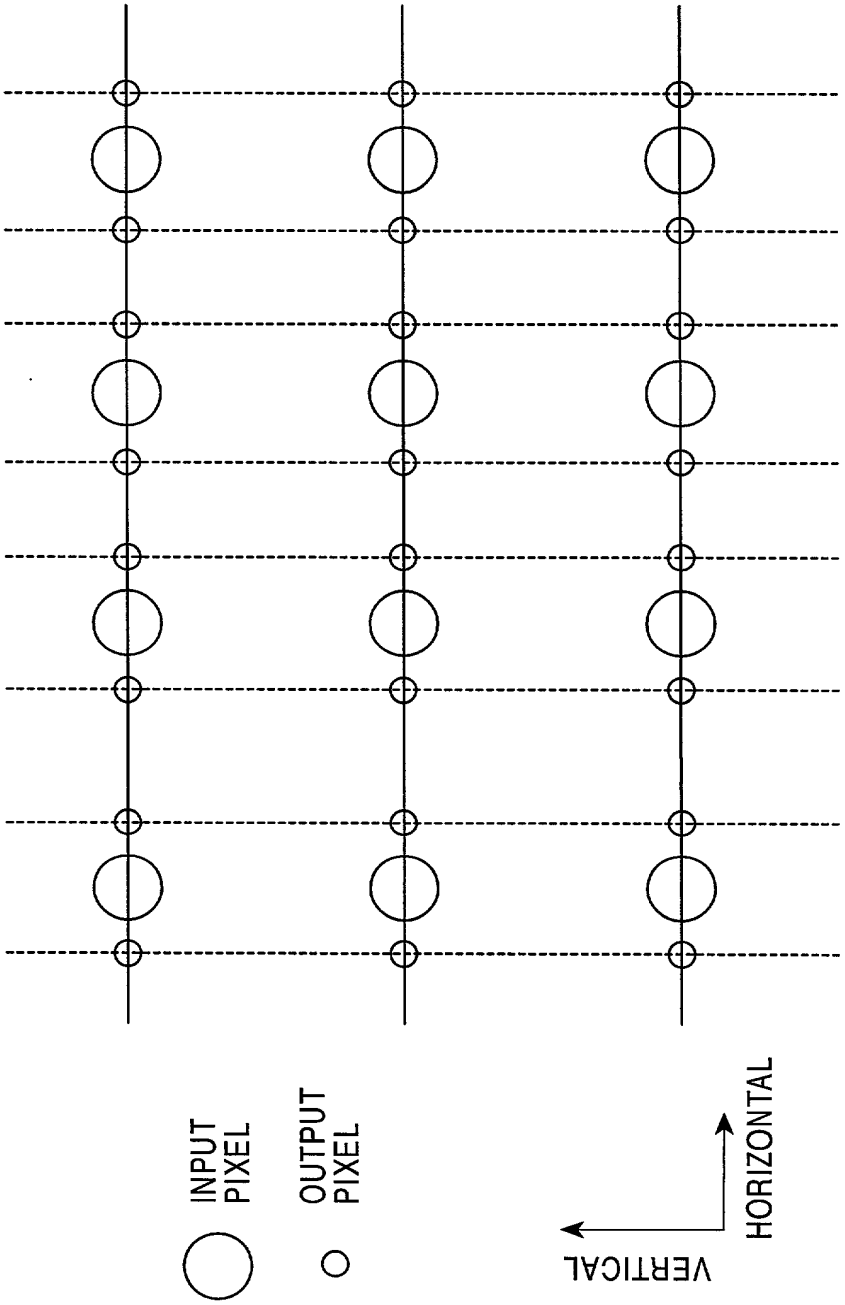


FIG. 66

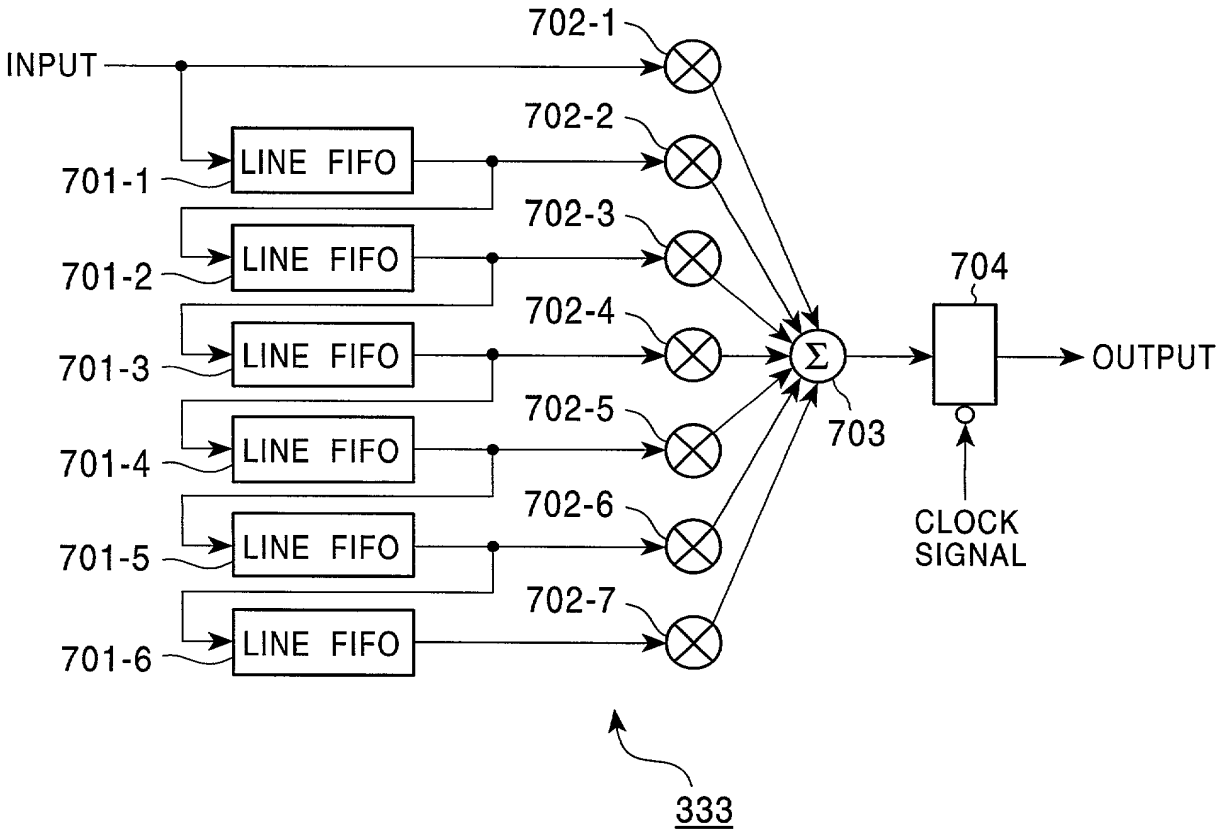

INPUT
LINE FIFO
701-1
701-2
701-3
701-4
701-5
701-6
702-1
702-2
702-3
702-4
702-5
702-6
702-7
Σ
703
704
OUTPUT
CLOCK SIGNAL
333

FIG. 67

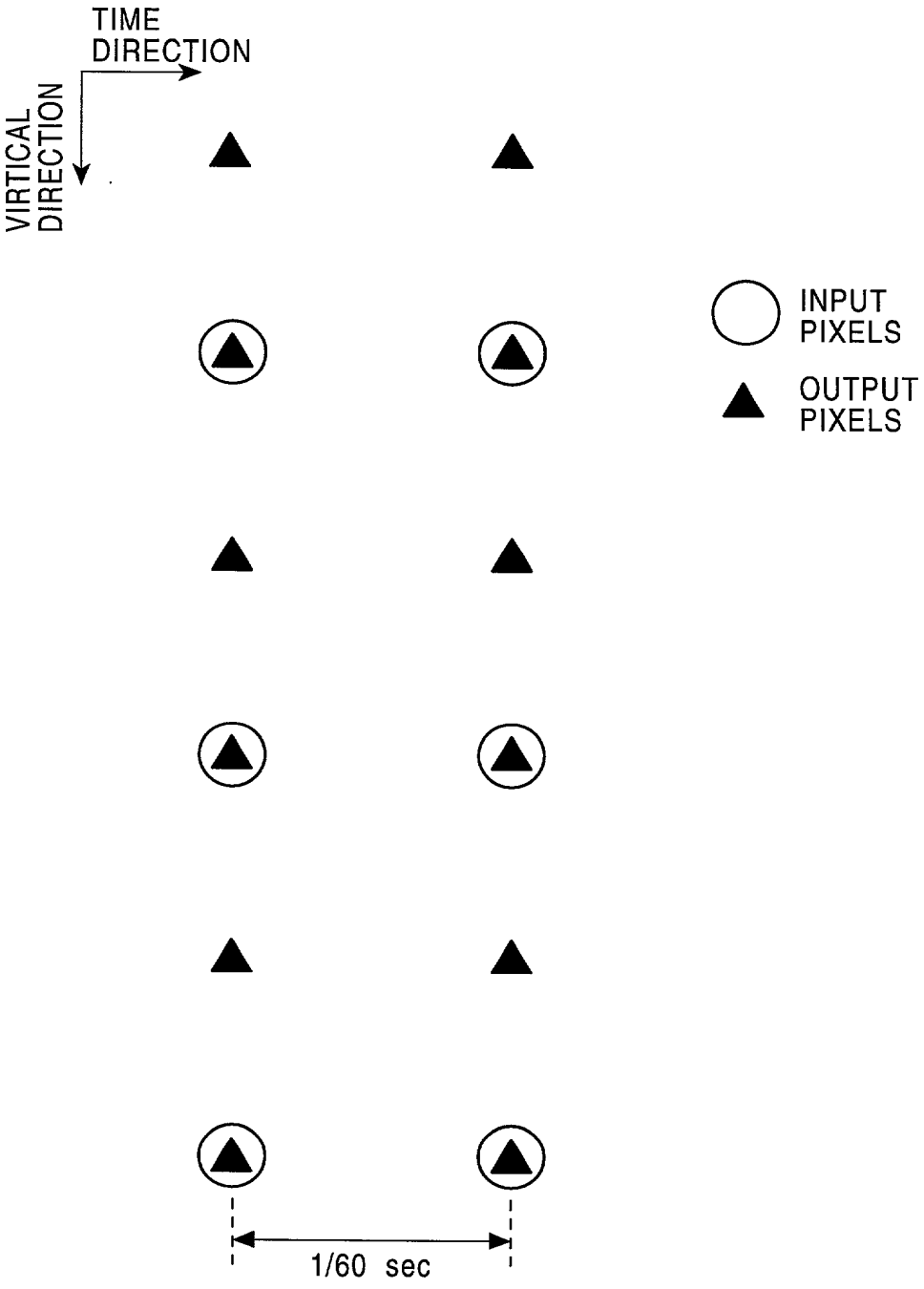

TIME DIRECTION
VIRTICAL DIRECTION
INPUT PIXELS
OUTPUT PIXELS
1/60 sec

FIG. 68

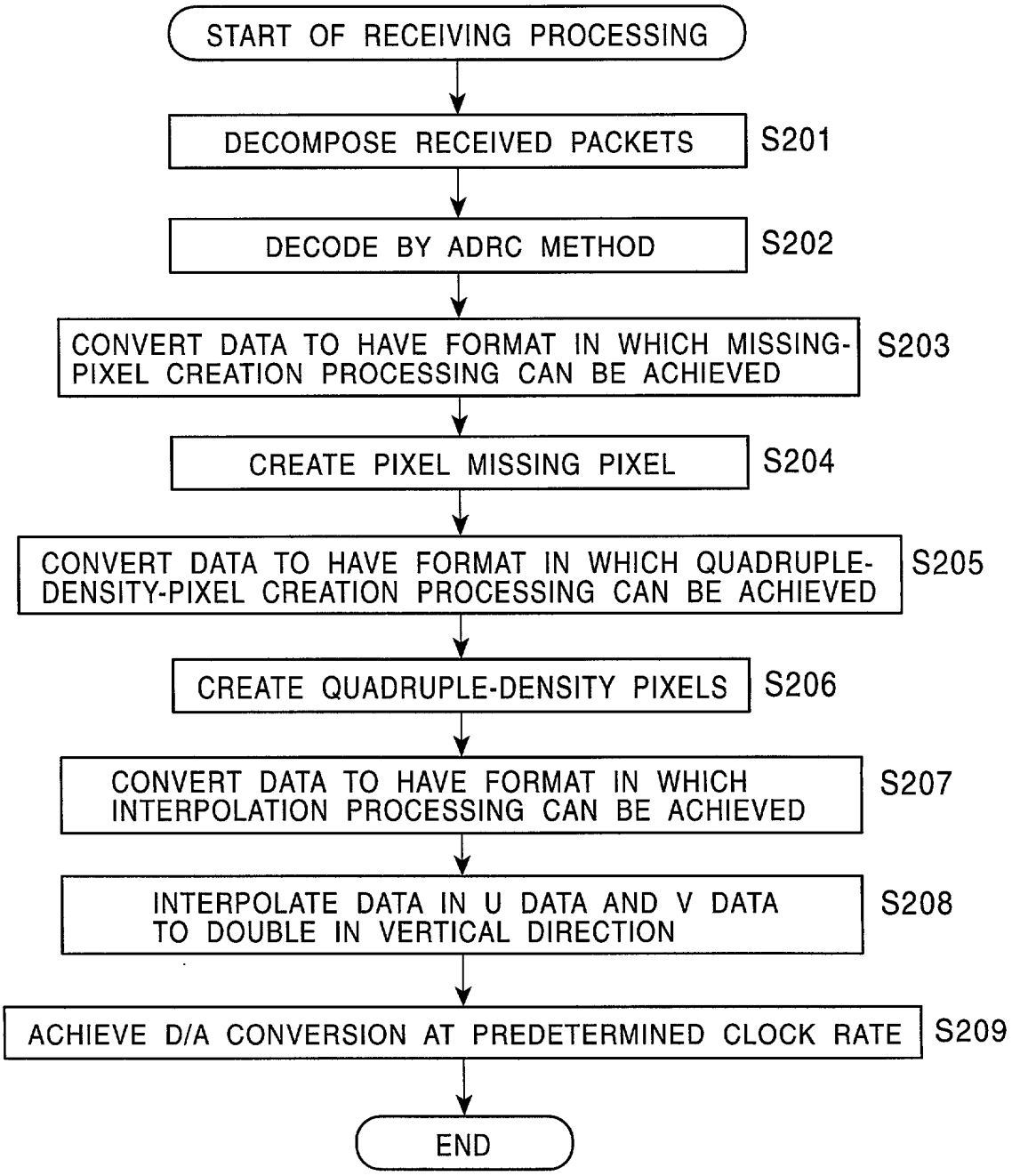

START OF RECEIVING PROCESSING
DECOMPOSE RECEIVED PACKETS
S201
DECODE BY ADRC METHOD
S202
CONVERT DATA TO HAVE FORMAT IN WHICH MISSING-PIXEL CREATION PROCESSING CAN BE ACHIEVED
S203
CREATE PIXEL MISSING PIXEL
S204
CONVERT DATA TO HAVE FORMAT IN WHICH QUADRUPLE-DENSITY-PIXEL CREATION PROCESSING CAN BE ACHIEVED
S205
CREATE QUADRUPLE-DENSITY PIXELS
S206
CONVERT DATA TO HAVE FORMAT IN WHICH INTERPOLATION PROCESSING CAN BE ACHIEVED
S207
INTERPOLATE DATA IN U DATA AND V DATA TO DOUBLE IN VERTICAL DIRECTION
S208
ACHIEVE D/A CONVERSION AT PREDETERMINED CLOCK RATE
S209
END

FIG. 69

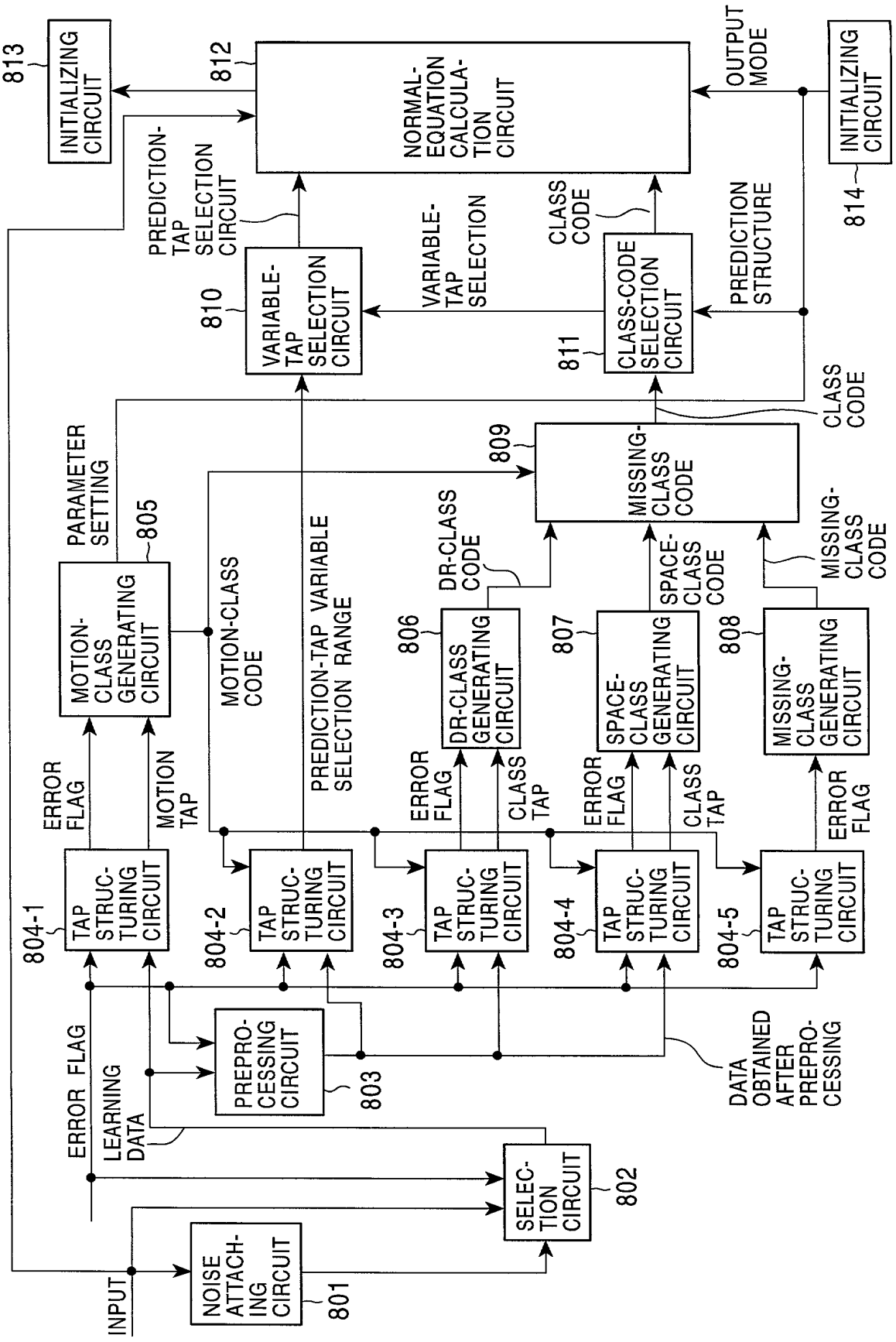

INPUT
NOISE ATTACHING CIRCUIT
801
SELECTION CIRCUIT
802
PREPROCESSING CIRCUIT
803
ERROR FLAG
LEARNING DATA
DATA OBTAINED AFTER PREPROCESSING
804-1
TAP STRUCTURING CIRCUIT
804-2
TAP STRUCTURING CIRCUIT
804-3
TAP STRUCTURING CIRCUIT
804-4
TAP STRUCTURING CIRCUIT
804-5
TAP STRUCTURING CIRCUIT
ERROR FLAG
MOTION TAP
ERROR FLAG
CLASS TAP
ERROR FLAG
CLASS TAP
ERROR FLAG
MOTION-CLASS GENERATING CIRCUIT
805
PARAMETER SETTING
MOTION-CLASS CODE
PREDICTION-TAP SELECTION RANGE
VARIABLE
DR-CLASS GENERATING CIRCUIT
806
DR-CLASS CODE
SPACE-CLASS GENERATING CIRCUIT
807
SPACE-CLASS CODE
MISSING-CLASS GENERATING CIRCUIT
808
MISSING-CLASS CODE
MISSING-CLASS CODE
809
CLASS CODE
VARIABLE-TAP SELECTION CIRCUIT
810
PREDICTION-TAP SELECTION CIRCUIT
VARIABLE-TAP SELECTION
CLASS-CODE SELECTION CIRCUIT
811
CLASS CODE
PREDICTION STRUCTURE
NORMAL-EQUATION CALCULATION CIRCUIT
812
OUTPUT MODE
INITIALIZING CIRCUIT
813
INITIALIZING CIRCUIT
814

FIG. 70

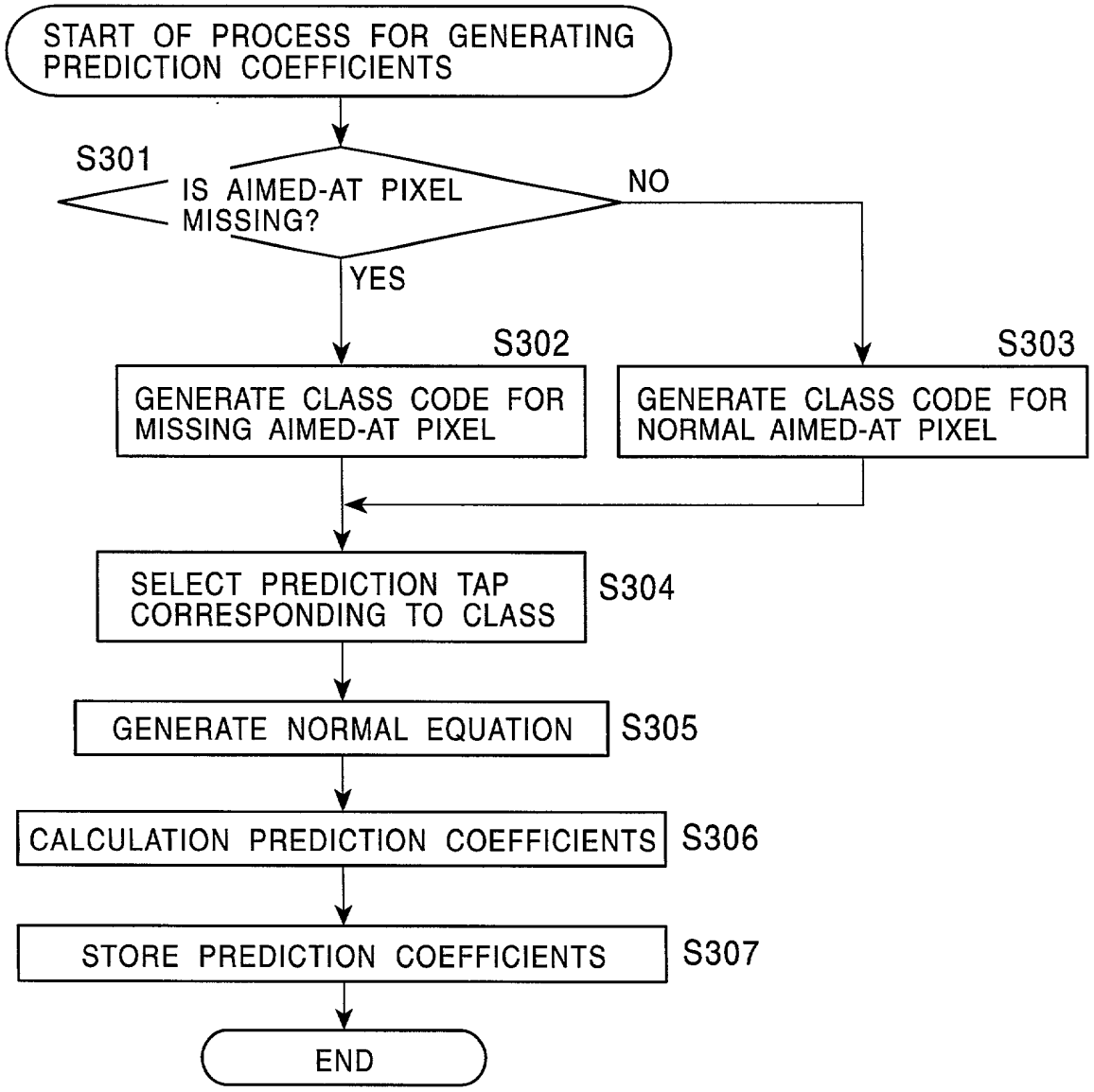
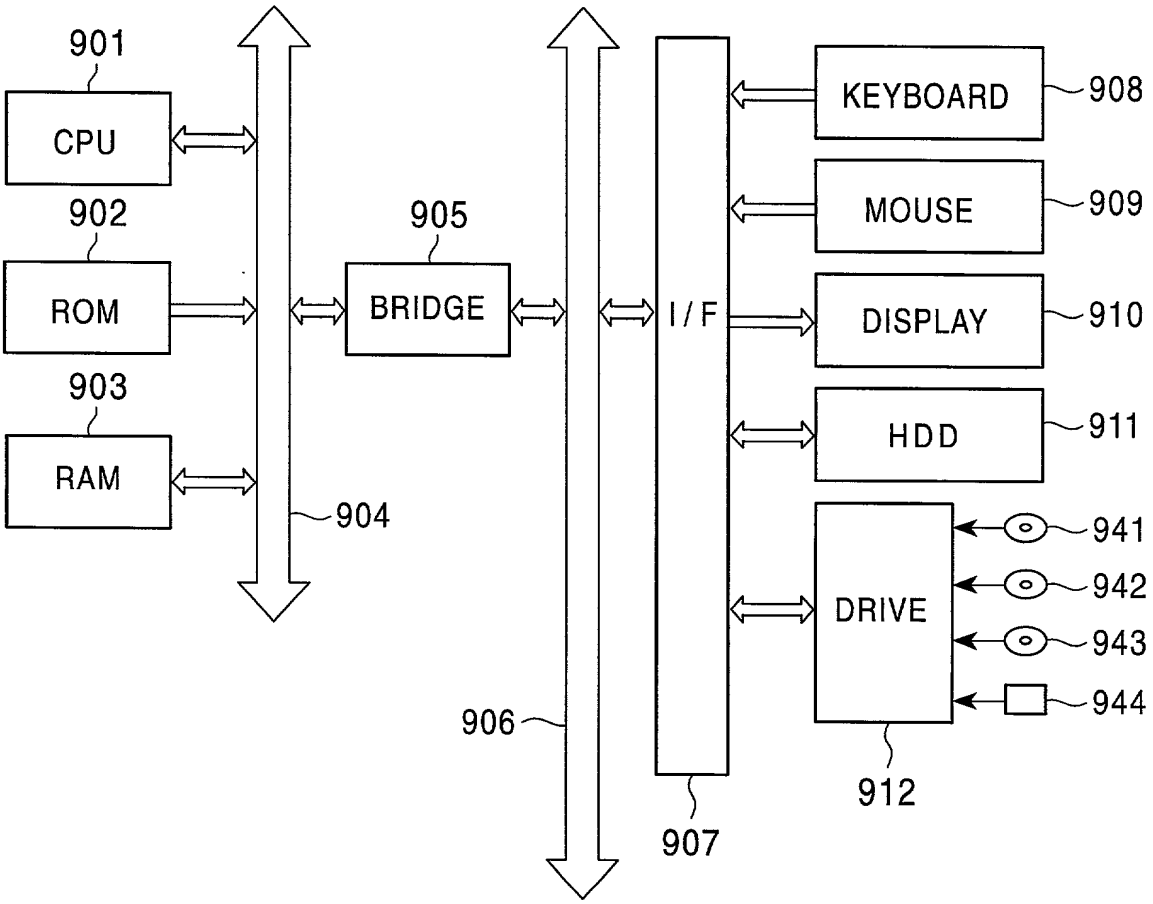

START OF PROCESS FOR GENERATING PREDICTION COEFFICIENTS
S301
IS AIMED-AT PIXEL MISSING?
NO
YES
S302
GENERATE CLASS CODE FOR MISSING AIMED-AT PIXEL
S303
GENERATE CLASS CODE FOR NORMAL AIMED-AT PIXEL
SELECT PREDICTION TAP CORRESPONDING TO CLASS
S304
GENERATE NORMAL EQUATION
S305
CALCULATION PREDICTION COEFFICIENTS
S306
STORE PREDICTION COEFFICIENTS
S307
END

FIG. 71


901
CPU
902
ROM
903
RAM
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